Badriprasad Institute of Technology, Sambalpur

Lesson plan for Theory -3,Digital Electronics & Microprocessor

Semester & Branch : 5th Sem , Electrical Engineering **Total Periods-75**

Name of the faculty : Swetanjali Nayak **No of periods /week-5**

WEEK	CLASS DAY	THEORY
1ST	1ST	BASICS OF DIGITAL ELECTRONICS- BINARY, OCTAL, HEXADECIMAL NUMBER SYSTEM
	2ND	COMPARE WITH DECIMAL NUMBER SYSTEM
	3RD	BINARY ADDITION, UBSTRACTION
	4TH	BINARY MULTIPLICATION, DIVISION
	5TH	1'S COMPLEMENT & 2'S COMPLEMENT NUMBERS FOR A BINARY NUMBER
2ND	1ST	SUBSTRACTION OF BINARY NUMBERS IN 2'S COMPLEMENT METHOD
	2ND	USE OF WEIGHTED AND NON-WEIGHTED CODES
	3RD	WRITE BINARY EQUIVALENT NUMBER FOR A NUMBER IN 8421, EXCESS-3 AND GRAY CODE AND VICE VERSA
	4TH	IMPORTANCE OF PARITY BIT
	5TH	LOGIC GATES- AND, OR, NOT, NAND GATES WITH TRUTH TABLE
3RD	1ST	NOR AND EX-OR GATES
	2ND	REALIZE AND, OR, NOT OPERATIONS USING NAND & NOR GATES
	3RD	DIFFERENT POSTULATES AND DEMORGAN'S THEOREM IN BOOLEAN ALGEBRA
	4TH	USE OF BOOLEAN ALGEBRA FOR SIMPLIFICATION OF LOGIC EXPRESSION
	5TH	KARNAUGH MAP FOR 2,3,4 VARIABLE, SIMPLIFICATION OF SOP & POS LOGIC EXPRESSION USING K-MAP
4TH	1ST	CONCEPT OF COMBINATIONAL LOGIC CIRCUITS
	2ND	HALF ADDER CIRCUIT AND VERIFY ITS FUNCTIONALITY USING TRUTH TABLE
	3RD	REALIZE A HALF ADDER USING NAND GATES ONLY & NOR GATES ONLY
	4TH	FULL ADDER CIRCUIT AND EXPLAIN ITS OPERATION WITH TRUTH TABLE
	5TH	REALIZE FULL ADDER USING TWO HALF ADDER
5TH	1ST	REALIZE FULL ADDER USING OR GATE & WRITE TRUTH TABLE
	2ND	FULL SUBSTRACTOR CIRCUIT & EXPLAIN ITS OPERATION WITH TRUTH TABLE
	3RD	OPERATION OF 4X1 MULIPLEXER
	4TH	OPERTION OF 1X4 DE-MULTIPLEXER
	5TH	WORKING OF BINARY-DECIMAL ENCODER
6TH	1ST	3X8 DECODER
	2ND	WORKING OF 2-BIT MAGNITUDE COMPARATOR
	3RD	IDEA OF SEQUENTIAL LOGIC CIRCUIT
	4TH	STATE THE NECESSITY OF CLOCK AND GIVE THE CONCEPT OF LEVEL CLOCKING AND EDGE TRIGGERING
	5TH	CLOCKED SR FLIP FLOP WITH PRSET AND CLEAR INPUTS
7TH	1ST	CONSTRUCT LEVEL CLOCKED JK FLIPFLOP USING SR FLIP FLOP AND EXPLAIN WITH TRUTH TABLE
	2ND	CONCEPT OF RACE AROUND CONDITION AND STUDY OF MASTER SLAVE JK FLIPFLOP
	3RD	TRUTH TABLES OF EDGE TRIGGERED D AND T FLIP FLOPS AND DRAW THEIR SYMBOLS
	4TH	APPLICATIONS OF FLIP FLOPS
	5TH	DEFINE MODULUS OF A COUNTER
8TH	1ST	4-BIT ASYNCHRONOUS COUNTER & TIMING DIAGRAM
	2ND	ASYNCHRONOUS DECADE COUNTER
	3RD	4 BIT SYNCHRONOUS COUNTER
	4TH	DISTINGUISH BETWEEN SYNCHRONOUS AND ASYNCHRONOUS COUNTER
	5TH	STATE THE NEED FOR A REGISTER AND LIST THE FOUR TYPES OF REGISTER

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9TH	1ST	WORKING OF SISO, SIPO REGISTER WITH TRUTH TABLE USING FLIP FLOP
	2ND	WORKING OF PISO, PIPO REGISTER WITH TRUTH TABLE
	3RD	8085 MICROPROCESSOR- INTRODUCTION TO MICROPROCESSOR & MICROCOMPUTER
	4TH	ARCHITECTURE OF INTEL 8085 MICROPROCESSOR
	5TH	DESCRIPTION OF EACH BLOCK
10TH	1ST	PIN DIAGRAM AND DESCRIPTION
	2ND	STACK, STACK PIONTER, STACK TOP
	3RD	INTERRUPTS
	4TH	OPCODE & OPERANDS
	5TH	DIFFERENTIATE BETWEEN ONE BYTE, TWO BYTE, THREE BYTE INSTRUCTION
11TH	1ST	INSTRUCTION SET OF 8085 MICROPROCESSOR
	2ND	INSTRUCTION SET OF 8085 MICROPROCESSOR
	3RD	ADDRESSING MODES
	4TH	FETCH CYCLE, MACHINE CYCLE
	5TH	INSTRUCTION CYCLE, T-STATES
12TH	1ST	TIMING DIAGRAM OF MEMORY READ, MEMORY WRITE
	2ND	I/O READ , I/O WRITE TIMING DIAGRAM
	3RD	TIMING DIAGRAM OF 8085 INSTRUCTION
	4TH	COUNTER & TIME DELAY
	5TH	SIMPLE SSEMBLY LANGUAGE PROGRAMMING OF 8085
13TH	1ST	INTERFACING AND SUPPORT CHIPS
	2ND	BASIC INTERFACING CONCEPTS
	3RD	MEMORY MAPPING
	4TH	I/O MAPPING
	5TH	FUNCTIONAL BLOCK DIAGRAM OF PROGRAMMABLE PERIPHERAL INTERFACE INTEL 8255
14TH	1ST	APPLICATION USING 8255- SEVEN SEGMENT LED DISPLAY
	2ND	SQUARE WAVE GENERATOR
	3RD	TRAFFIC LIGHT CONTROLLER
	4TH	OBJECTIVE TYPE QUESTION DISCUSSION
	5TH	OBJECTIVE TYPE QUESTION DISCUSSION
15TH	1ST	SEMESTER PATTERN QUESTION DISCUSSION
	2ND	SEMESTER PATTERN QUESTION DISCUSSION
	3RD	PRACTICE TEST-1
	4TH	PRACTICE TEST-2
	5TH	PRACTICE TEST-3

(SIGNATURE OF FACULTY) **(SIGNATURE OF HOD**