Badriprasad Institute of Technology, Sambalpur

Lesson plan for Theory -2, VLSI & EMBEDDED SYSTEM

Semester & Branch : 5TH SEM, ETC Engineering **Total Periods-60**

Name of the faculty : MR. SARTHAK PANDA **No of periods /week-4**

WEEK	CLASS DAY	THEORY
1ST	1ST	INTRODUCTION TO VLSI
	2ND	CLASSIFICATION OF CMOS DIGITAL CIRCUIT TYPES
	3RD	INTRODUCTION TO MOS TRANSISTOR, BASIC OPERATION OF MOSFET
	4TH	STRUCTURE AND OPERATION OF MOSFET,CMOS
2ND	1ST	V-I CHARACTERISTICS OF MOSFET
	2ND	WORKING OF MOSFET CAPACITANCE
	3RD	MODELLING OF MOS TRANSISTORS ,SPICE LEVEL-1,LEVEL 2 AND LEVEL 3
	4TH	FLOW CIRCUIT DESIGN PROCEDURES
3RD	1ST	VLSI DESIGN FLOW & Y CHART
	2ND	DESIGN HIERARCHY
	3RD	VLSI DESIGN STYLES-FPGA,GATE ARRAY DESIGN
	4TH	VLSI DESIGN STYLES-STANDARD CELLS BASED,FULL CUSTOM
4TH	1ST	SIMPLIFIED PROCESS SEQUENCE FOR FABRICATION
	2ND	BASIC STEPS IN FABRICATION PROCESSES FLOW
	3RD	FABRICATION PROCESS OF nMOS TRANSISTOR
	4TH	CMOS n-WELL FABRICATION PROCESS FLOW
5TH	1ST	MOS FABRICATION PROCESS BY n-WELL ON P-SUBSTRATE
	2ND	LAYOUT DESIGN RULES
	3RD	STICK DIAGRAMS OF CMOS INVERTER
	4TH	STICK DIAGRAMS OF CMOS INVERTER
6TH	1ST	BASIC n-MOS INVERTERS
	2ND	WORKING OF RESISTIVE -LOAD INVERTER
	3RD	INVERTER WITH n-TYPE MOSFET LOAD-ENHANCEMENT LOAD
	4TH	DEPLETION n-MOS INVERTER
7TH	1ST	C-MOS INVERTER OPERATION, CHARACTERISTICS AND INTERCONNECT EFFECTS:DELAY TIME
	2ND	C-MOS INVERTER OPERATION, CHARACTERISTICS AND INTERCONNECT EFFECTS:DELAY TIME
	3RD	CMOS INVERTER DESIGN WITH DELAY CONSTRAINTS
	4TH	TWO SAMPLE MASK LAYOUT FOR P-TYPE SUBSTRATE
8TH	1ST	STATIC COMBINATIONAL LOGIC WORKING OF STATIC CMOS LOGIC CIRCUITS
	2ND	CMOS LOGIC CIRCUITS(NAND2 GATE)
	3RD	CMOS TRANSMISSION GATES (PASS GATE)
	4TH	BASIC COMPLEX LOGIC CIRCUITS
9TH	1ST	CLASSIFICATION OF LOGIC CIRCUITS BASED ON THEIR TEMPORAL BEHAVIOUR
	2ND	SR FLIP LATCH CIRCUIT
	3RD	CLOCKED SR LATCH
	4TH	CMOS D LATCH
10TH	1ST	BASIC PRINCIPLE OF DYNAMIC PASS TRANSISTOR CIRCUITS
	2ND	DYNAMIC RAM,SRAM
	3RD	FLASH MEMORY
	4TH	SPL & HDL DESIGN LANGUAGE
11TH	1ST	HDL & EDA TOOLS &VHDL AND XLINX PACKAGES
	2ND	DESIGN STRATEGIES & CONCEPT OF FPGA WITH STANDARD CELL BASED DESIGN
	3RD	VHDL FOR DESIGN SYNTHESIS USING CPLD
	4TH	VHDL FOR DESIGN SYNTHESIS USING FPGA
12TH	1ST	RASPBERRY Pi BASIC IDEA
	2ND	EMBEDDED SYSTEMS OVERVIEW,LIST OF EMBEDDED SYSTEMS

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	3RD	CHARACTERISTICS OF EMBEDDED SYSTEM EXAMPLE DIGITAL CAMERA
	4TH	TECHNOLOGY FOR EMBEDDED SYSTEM
13TH	1ST	PROCESSOR TECHNOLOGY
	2ND	IC TECHNOLOGY
	3RD	DESIGN TECHNOLOGY-PROCESSOR TECHNOLOGY GENERAL PURPOSE PROCESSORS SOFTWARE
	4TH	BASIC ARCHITECTURE OF SINGLE PURPOSE PROCESSOR HARDWARE
14TH	1ST	APPLICATION,SPECIFIC PROCESSOR,MICROCONTROLLERS,DSP
	2ND	FULL CUSTOM IC DESIGN
	3RD	SEMICUSTOM IC DESIGN
	4TH	PLD(PROGRAMMABLE LOGIC DEVICE)
15TH	1ST	BASIC IDEA OF ARDUINO MICRO CONTROLLER
	2ND	OBJECTIVE TYPES QUESTION DISCUSSION
	3RD	SEMESTER PATTERN QUESTION DISCUSSION
	4TH	PRACTICE TEST

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