[CHAPTER-1]

-------------------------------- [DIODE & CIRCUITS] --------------------------------

CONSTRUCTION & WORKING PRINCIPLE OF DIODE: -

- When a p-type semiconductor is suitably joined to n-type semiconductor, the contact surface is called **PN Junction**. Most semiconductor devices contain one or more PN junctions.
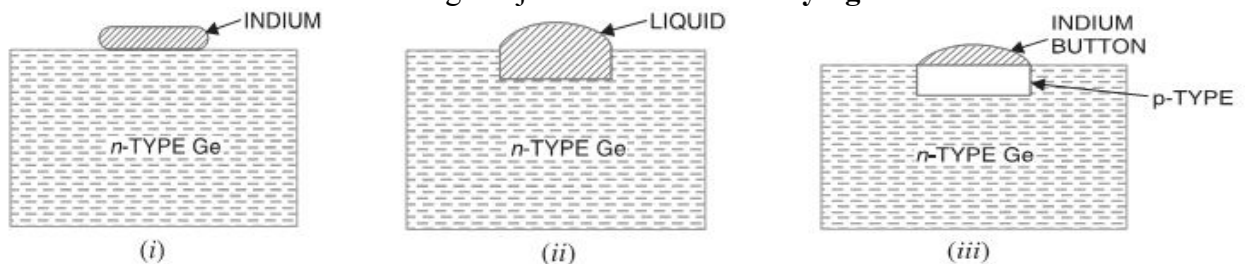
Formation of PN junction.

- In actual practice, the characteristic properties of PN junction will not be apparent if a p-type block is just brought in contact with n-type block. In fact, it is **fabricated** by special techniques.
- There are a number of techniques for the fabrication of PN-Junction: -
    - ♣ Grown Junction
    - ♣ Alloy Junction
    - ♣ Diffused Junction
    - ♣ Epitaxial Growth
    - ♣ Point contract Junction.
- But the most common method of making PN junction is called **Alloying**.

[Figures of different stages of formation of PN junction by Alloying method **]**

- In this method, a small block of indium (trivalent impurity) is placed on an n-type germanium slab as shown in Fig (i). The system is then heated to a temperature of about 500ºC.
- The indium and some of the germanium melt to form a small puddle of molten germanium-indium mixture as shown in Fig (ii).
- The temperature is then lowered and puddle begins to solidify. Under proper conditions, the atoms of indium impurity will be suitably adjusted in the germanium slab to form a single crystal. Addition of indium overcomes the excess of electrons in the n-type germanium to such an extent that it creates a p-type region. As the process goes on, the remaining molten mixture becomes increasingly rich in indium.
- When all germanium has been redeposited, the remaining material appears as indium button which is frozen on to the outer surface of the crystallized portion as shown in Fig. (iii).

Properties of PN Junction.

- To explain PN junction, consider two types of materials: - 1) P-Type & 2) N-Type.
- P-type semiconductor having –ive acceptor ions and +ive charged holes. N-type semiconductor having +ive donor ions & –ive free electrons.
- P-type has high concentration of holes and N-type has high concentration of electrons.
- So there is a tendency for the free electron to diffuse over p-side and holes to n-side. This process is called **Diffusion.**
- When a free electron move across the junction from n-type to p-type, positive donor ions are removed by the force of electrons. Hence positive charge is built on the n-side of the junction.
- Similarly negative charge establish on p-side of the junction.
- When sufficient no of donor and accepter ions gathered at the junction, further diffusion prevented. Because +ive charge on n-side repel holes to cross from p-side to n-side, similarly –ive charge on p-side repel free electrons to cross from n-type to p-type.
- Thus a barrier is set up against further movement of charge carriers is hole or electrons. This barrier is called as **Potential Barrier/ Junction Barrier (V_0)** and is of the order 0.1 to 0.3 volt. This prevents the respective majority carriers for crossing the barrier region. This region is known as **Depletion Layer**
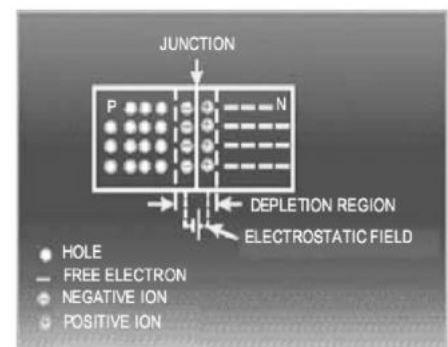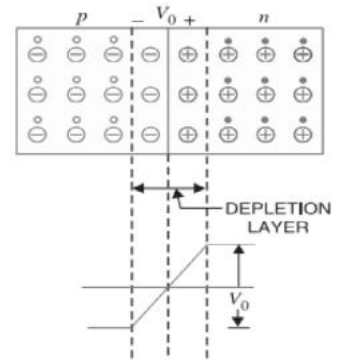
➤ The term depletion is due to the fact that near the junction, the region is depleted (i.e. emptied) of charge carries (free electrons and holes) due to diffusion across the junction.

➤ It may be noted that depletion layer is formed very quickly and is very thin compared to the n-region and the p-region.
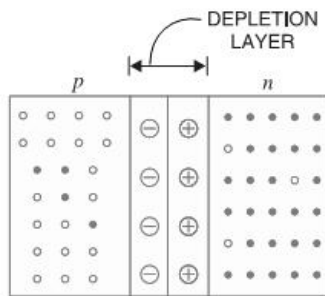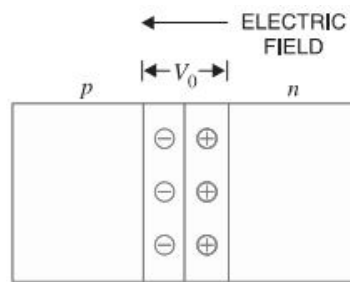
➤ Once pn junction is formed and depletion layer created, the diffusion of free electrons stops. In other words, the depletion region acts as a barrier to the further movement of free electrons across the junction. The positive and negative charges set up an electric field as shown in the fig above.

➤ The electric field is a barrier to the free electrons in the n-region. There exists a potential difference across the depletion layer and is called Barrier Potential (V_0).

➤ The barrier potential of a pn junction depends upon several factors including the type of semiconductor material, the amount of doping and temperature.

➤ The typical barrier potential is approximately: - For Silicon, $V_0 = 0.7$ V ; For Germanium, $V_0 = 0.3$ V

❖ Junction Capacitance:-

➤ When a PN junction is formed, a layer of positive and negative impurity ions is formed on either side of the pn junction. This depletion layer acts as dielectric (non-conductive) medium between P-region and N-region. Therefore, these regions act as two plates of a capacitor separated by dielectric medium.

➤ The capacitance formed in this junction is called as Depletion Layer Capacitance or Space Charge Capacitance or Transition Region Capacitance or simple **Junction Capacitance.**

✚ Applying D.C. Voltage Across PN Junction or Biasing a PN Junction

➤ In electronics, the term bias refers to the use of D.C. voltage to establish certain operating conditions for an electronic device. In relation to a PN junction, there are following two bias conditions :
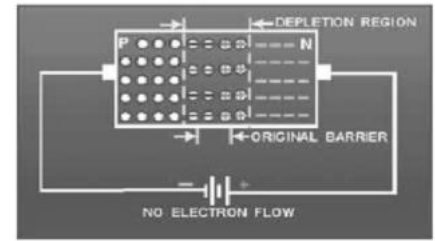
1. Forward Biasing **2.** Reverse Biasing

❖ Forward Biasing.
When external D.C. voltage applied to the junction is in such a direction that it cancels the potential barrier, thus permitting current flow, it is called **Forward Biasing**.

➤ To apply forward bias, connect positive terminal of the battery to p-type and negative terminal to n-type as shown in Fig.

➤ The applied forward potential establishes an electric field which acts against the field due to potential barrier.

➤ Therefore, the resultant field is weakened and the barrier height is reduced at the junction.

➤ As potential barrier voltage is very small (0.1 to 0.3 V), therefore, a small forward voltage is sufficient to completely eliminate the barrier.

➤ Once the potential barrier is eliminated by the forward voltage, junction resistance becomes almost zero and a low resistance path is established for the entire circuit.

➤ Thus, current flows in the circuit. This is called **Forward Current**.

➤ With forward bias to PN junction, the important points are: -

(i) The potential barrier is reduced and at some forward voltage i. e. (0.1 to 0.3 V), it is eliminated altogether.

(ii) The junction offers low resistance (forward resistance, R_f) to current flow.

(iii) Current flows in the circuit due to the establishment of low resistance path.

(iv) The magnitude of current depends upon the applied forward voltage.
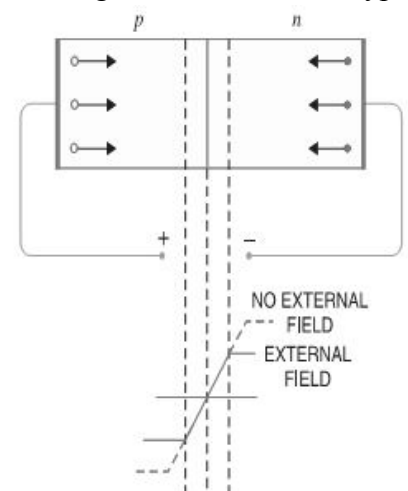
❖ **Reverse Biasing.** When the external D.C. voltage applied to the junction is in such a direction that potential barrier is increased, it is called **Reverse Biasing.**
  ➢ For reverse bias, connect -ve terminal of battery to p-type and +ve terminal to n-type as shown in Fig.
  ➢ It is clear that applied reverse voltage establishes an electric field which acts in the same direction as the field due to potential barrier.
  ➢ Therefore, the resultant field at the junction is strengthened and the barrier height is increased as shown in Fig.
  ➢ The increased potential barrier prevents the flow of charge carriers across the junction. Thus, a high resistance path is established for the entire circuit and hence the current does not flow.
♣ With reverse bias to PN junction, The important points are:
   (i) The potential barrier is increased.
   (ii) The junction offers very high resistance R_r) to current flow.
   (iii) No current flows in the circuit due to high resistance path.
  ➢ **Conclusion: -** From the above discussion, it follows that with reverse bias to the junction, a high resistance path is established and hence no current flow occurs.
  ➢ Whereas with forward bias to junction low resistance path is set up & hence current flows in the circuit.
❖ **Current Flow in a Forward Biased PN Junction:-**
  ➢ It concluded that in n-type region, current carried by free electrons whereas in p-type region, it is carried by holes. However, in external connecting wires, current is carried only by free electrons.
⚓ **Volt-Ampere Characteristics of PN Junction:-**
  ➢ Volt-ampere or V-I characteristic of a pn junction (also called a crystal or semiconductor diode) is the curve between voltage across the junction and the circuit current.
  ➢ Usually, voltage is taken along x-axis and current along y-axis. Fig. shows the circuit arrangement for determining the V-I characteristics of a pn junction.
  ➢ The characteristics can be studied under three heads, namely: -
   **(1)** Zero external voltage, **(2)** Forward Bias **(3)** Reverse Bias.
❖ **(i) Zero external voltage: -** When the external voltage is zero, i.e. circuit is open at K; the potential barrier at the junction does not permit current flow. Therefore, the circuit current is zero as indicated by point O in Fig.
  ➢ **(ii) Forward Bias**: - With forward bias to the pn junction i.e. p-type connected to positive terminal and n-type connected to negative terminal, the potential barrier is reduced. At some forward voltage (0.7 V for Si and 0.3 V for Ge), the potential barrier is altogether eliminated and current starts flowing in the circuit. From now onwards, the current increases with the increase in forward voltage.
  ➢ Thus, a rising curve OB is obtained with forward bias as in Fig. From the forward characteristic, it is seen that at first (region OA), the current increases very slowly and the curve is non-linear. Because the external applied voltage is used up in overcoming the potential barrier.
 ➢ Once external voltage exceeds potential barrier voltage, the pn junction behaves like ordinary conductor.
  ➢ Therefore, the current rises very sharply with increase in external voltage (region AB on the curve). The curve is almost linear.
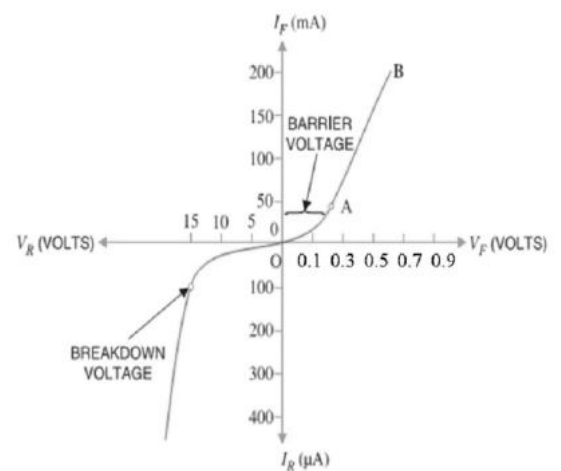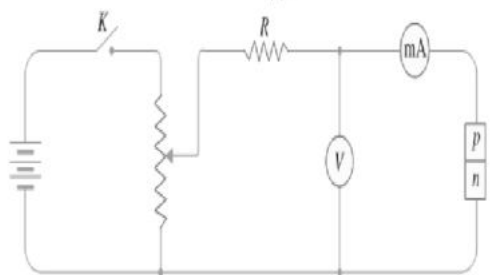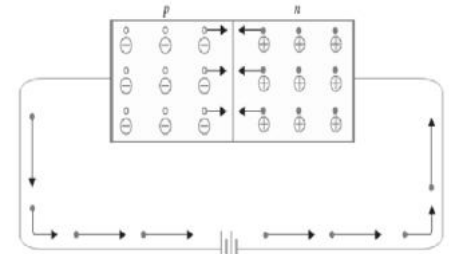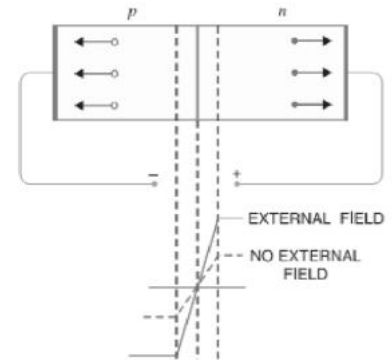
❖ **(iii) Reverse Bias: -** With reverse bias to the pn junction i.e. p-type connected to negative terminal and n-type connected to positive terminal, potential barrier at the junction is increased. Therefore, the junction resistance becomes very high and practically no current flows through the circuit.

➢ However, in practice, a very small current (of the order of µA) flows in the circuit with reverse bias as shown in the reverse characteristic.

➢ This is called **Reverse Saturation Current** (Is) and is due to the minority carriers.

➢ It may be recalled that there are a few free electrons in p-type material and a few holes in n-type material.

➢ These undesirable free electrons in p-type and holes in n-type are called minority carriers. As shown in side Fig. to these minority carriers, the applied reverse bias appears as forward bias.

➢ Therefore, a small current flows in the reverse direction. If reverse voltage is increased continuously, the kinetic energy of electrons (minority carriers) may become high enough to knock out electrons from the semiconductor atoms.

➢ At this stage breakdown of the junction occurs, characterized by a sudden rise of reverse current and a sudden fall of the resistance of barrier region. This may destroy the junction permanently.

➢ **Note: -**The forward current through a pn junction is due to the majority carriers produced by the impurity. However, reverse current is due to the minority carriers produced due to breaking of some co-valent bonds at room temperature.
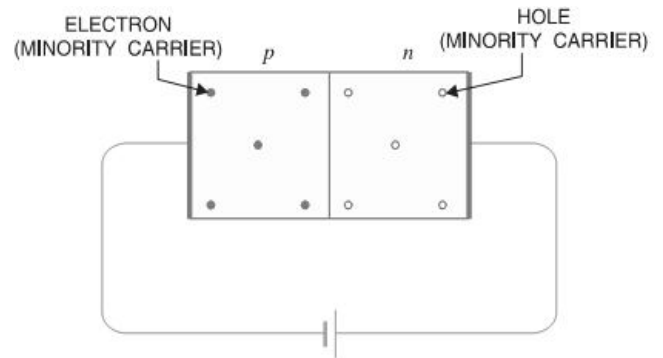
❖ **Important Terms: -**

(i) Breakdown Voltage: - It is the minimum reverse voltage at which pn junction breaks down with sudden rise in reverse current.

(ii) Knee Voltage: - The forward voltage at which the current through the junction starts to increase rapidly.

(iii) Peak inverse voltage (PIV):- It is the maximum reverse voltage that can be applied to the pn junction without damage to the junction. If the reverse voltage across the junction exceeds its PIV, the junction may be destroyed due to excessive heat. The peak inverse voltage is of particular importance in rectifier service.

(iv) Maximum forward current: - It is the highest instantaneous forward current that a pn junction can conduct without damage to the junction. Manufacturer's data sheet usually specifies this rating. If the forward current in a pn junction is more than this rating, the junction will be destroyed due to overheating.

(v) Maximum power rating: - It is the maximum power that can be dissipated at the junction without damaging it. The power dissipated at the junction is equal to the product of junction current and the voltage across the junction
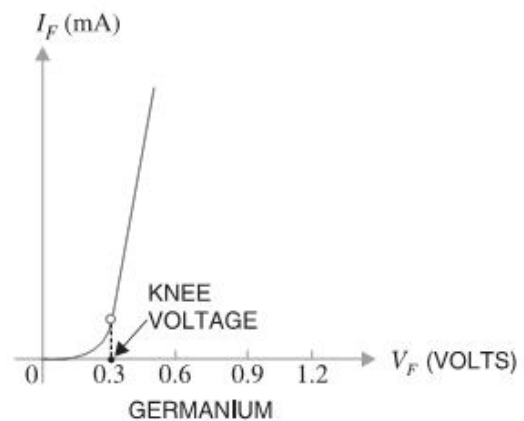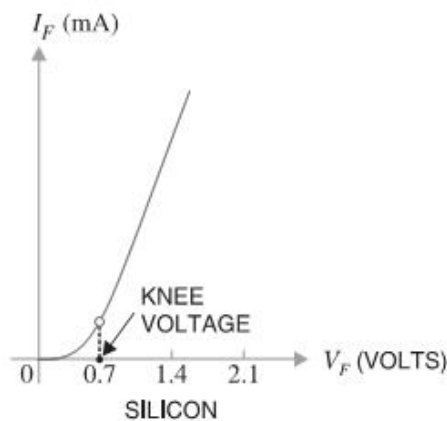
🔸 **Other Type of DIODES: -**

1.	Zener Diode	2.	Light Emitting Diode	3.	Tunnel Diode	4.	PIN Diodes
5.	Photo-Diode	6.	Varactor Diodes	7.	Laser Diodes	8.	Gunn Diodes
9.	Peltier diodes	10.	Step Recovery Diodes	11.	Schottky Diode	12.	Super Barrier Diodes
13.	Optoisolator	14.	Point-contact diodes	15.	Avalanche diodes	16.	Constant current diodes

🔸 **DIODE CURRENT EQUATION: -**

- The Mathematical equation, which describes the forward and reverse characteristics of a semiconductor diode is called the diode current equation.
- Let   I = Forward or Reverse Diode Current,

  I_0 = Reverse Saturation Current

  V = External Voltage. (It is +Ve for Forward Bias, -Ve or Reverse Bias)

  η = A constant, whose value is equal to 1 for Ge diode and 2 for Si diode for relatively low value of diode current (i.e. at or below the knee of the curve) and ή = 1 for Ge & Si diode for higher levels of diode current. (i. e. in the rapidly increasing section of the curve)

  V_T = Volt-equivalent of temperature. Its value is given by the relation T/11,600, where T is the absolute temperature. At room temperature (i.e. 300K), V_T = 26vmV.

- The current equation for a forward biased diode is given by the relation,

$$I = I_0 \left(e^{V/\eta \cdot V_T} - 1\right)$$

We know that at room temperature, V_T = 26mV = 0.026V. Substituting the value of V_T in the above equation it becomes,

$$I = I_0 \left(e^{40V/\eta} - 1\right)$$

- Thus diode current at or below the knee of the curve for Germanium and Silicon is given by

$$I_{Ge} = I_0 \left(e^{40V} - 1\right) \quad \textbf{[As } \boldsymbol{\eta} \textbf{= 1 for Ge]}$$

$$I_{Si} = I_0 \left(e^{20V} - 1\right) \quad \textbf{[As } \boldsymbol{\eta} \textbf{= 1 for Si]}$$

- If the value of applied voltage is greater than unity (i.e. for the diode current in the rapid by increasing section of the curve) then the equation of diode current for Germanium or Silicon is given by

$$I = I_0 \left(e^{40V} - 1\right) \quad \textbf{[As } \boldsymbol{\eta} \textbf{= 1 for Higher Value of Voltage]}$$

- The current equation for a reverse biased diode may be obtained by changing the sign of the applied voltage (V), i.e.

$$I = I_0 \left(e^{-V/\eta \cdot V_T} - 1\right)$$

- If the Value of V>>V_T, then the term $-V/\eta \cdot V_T$ << 1. Therefore $I = I_0$.
- Thus the diode current under reverse bias is equal to the reverse saturation current as long as the external voltage is below its break down value.

⊕ DIODE SPECIFICATION SHEET: -

- All manufactures of the semiconductor device provide data on specific diodes for the users to make proper utilization of the devices. This data could be a brief description limited to a one page or more than that. It includes the information arranged in table, graphs etc. The data is usually for : -
  - ♣ Forward voltage, V_F (At a specific Current & Temperature)
  - ♣ Maximum forward current, I_F (At a specific Temperature)
  - ♣ Reverse saturation current I_R or I_O (At a specific Voltage & Temperature)
  - ♣ Reverse Voltage Rating [PIV, PRV, VRRM or V(BR)], Where, BR=Breakdown at a specific current & temperature.
  - ♣ Maximum power dissipation level at a particular temperature.
  - ♣ Capacitance Value.
  - ♣ Reverse recovery time, t_{rr}.
  - ♣ Operating temperature range.
- Beside this, depending on the type of diode being considered, more data may also be provided such as frequency range, noise level, switching time, thermal resistance level and peak repetitive values.
- For the application in mind, the significance of the data will usually be self apparent.
- If the maximum power or dissipation rating is also provided, it is understood to be equal to the produce

$$P_{Dmax} = V_D I_D$$

  Where I_D and V_D are the diode current and voltage at a particular point of operation.

⊕ DIODE APPLICATIONS:

- A PN junction diode has an important characteristic that it conducts well in forward direction and poorly in reverse direction. This characteristic makes a diode very useful in a number of applications given below:
    1. As Rectifiers or Power Diodes in D.C. power supply.
    2. As Signal Diodes in communication circuits.
    3. As Zener Diodes in voltage stabilizing circuits.
    4. As Varactor Diodes in radio and TV receivers.
   5. As a Switch in logic circuits used in computers

✦ EFFECT OF TEMPERATURE OF DEPENDENCE OF JUNCTION DIODE:

- We have already discussed in the last article that the diode current is a function of temperature and the temperature appears in the denominator of the exponent term of the diode current equation (i.e., V/η . V_T is equal to $T/11600$).

- It is thus obvious that with the increase in temperature, the exponent will reduce and hence the diode current should also decrease.

- However, it has been found that the variation of saturation current (I_0) is much greater than the exponential term.

- The above fact may be expressed in the form of a mathematical relation as given below:

    Let, I_{01} = Saturation current at temp (T_1) for Ge or Si diode,

   & I_{02} = Saturation current at some other temperature (T_2)

    Then

    $$I_{02} = I_{01} . 2^{(T2 - T1)/10}$$
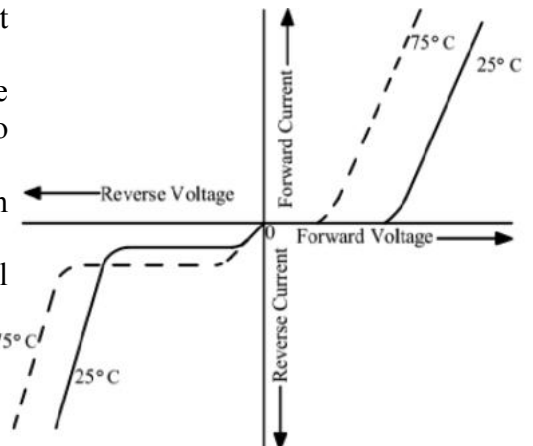
- As discussed in last chapter the reverse saturation current (I_0) will be just about double in magnitude for every 10ºC increase in temperature.

- For example, a germanium diode with an I_0 in the order of 1 or 2μ A at 25ºC has a leakage current of 100μ A (= 0.1 mA) at a temperature of 100ºC.

- Current levels of this magnitude in the reverse bias region would certainly question our desired open-circuit condition in the reverse bias region.

- However, typical values of I_0 for silicon diode are much lower than that of germanium for similar power and current levels.

- The increasing level of I_0 with temperature account for the lower threshold voltage as shown in Fig.

- Due to this reason forward characteristic at 75ºC is shown to the left to that of the characteristic at 25ºC.

- As the temperature increases, the forward characteristic shifts more and more to the left of the characteristic at 25ºC (i.e. become more and more "ideal").

- However, temperature beyond the normal operating range can have a very detrimental effect on the diode's maximum power and current levels.

- We see in Fig., that in the reverse bias region, the breakdown voltage is increasing with the increase in temperature.

✦ ZENER BREAK DOWN

- ♣ It has already been discussed that when the reverse bias on a crystal diode is increased, a critical voltage, called **Breakdown Voltage** is reached where the reverse current increases sharply to a high value.

- ♣ The breakdown region is the knee of the reverse characteristic as shown in Fig. The satisfactory explanation of this breakdown of the junction was first given by the American scientist C. Zener.

- ♣ The breakdown voltage is also called **Zener Voltage** or **Zener Break Down** & the sudden increase in current is known as **Zener Current**.

- ♣ The breakdown or Zener voltage depends upon the amount of doping.

- ♣ If the diode is heavily doped, depletion layer will be thin and consequently the breakdown of junction will occur at lower reverse voltage where as lightly doped diode has a higher breakdown voltage.
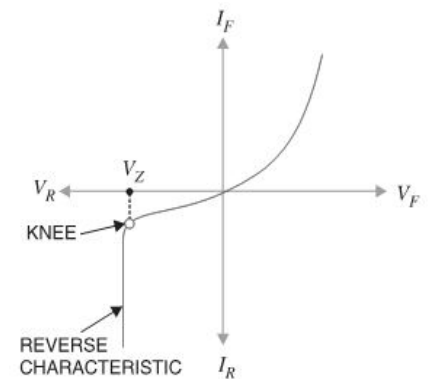
✦ AVALANCHE BREAKDOWN: -

♣ In this case the increased reverse voltage increases the amount of energy imparted to minority carriers.

♣ As the reverse voltage is increased further the minority carriers acquires a large amount of energy.

♣ When these carriers collide with Si or Ge atoms, within the crystal structure, they impart sufficient energy to break a covalent bond and generate additional carriers (electron-hole pair).

♣ These additional carriers pick up energy from the applied voltage and generates still more carriers. As a result of this, the reverse current increases rapidly.

♣ This cumulative process of carrier generation (multiplication) is known as **Avalanche Break down** or Avalanche **Multiplication**

❖ VARACTOR DIODE

➢ A junction diode which acts as a variable capacitor under changing reverse bias is known as a **varactor diode**. It is also known as **Varicap** or **Voltcap.**

➢ When a pn junction is formed, depletion layer is created in the junction area.

➢ Since there are no charge carriers within the depletion zone, the zone acts as an insulator.

➢ The p-type material with holes (+ive charge) as majority carriers and n-type material with electrons (−ive charge) as majority carriers act as charged plates.

➢ Thus the diode may be considered as a capacitor with n-region and p-region forming oppositely charged plates and with depletion zone between them acting as a dielectric.

➢ A varactor diode is specially constructed to have high capacitance under reverse bias.

➢ The values of capacitance of varactor diodes are in the pico farad (10^{-12} F) range.

➢ In normal operation, a varactor diode is always reverse biased.

➢ The capacitance of varactor diode is found as:

$$C_T = \varepsilon\, A/W_d$$

Where,

C_T = Total capacitance of the junction,
A = Cross-sectional area of the junction,
ε = Permittivity of the semiconductor material,
Wd = Width of the depletion layer.

➢ When reverse voltage across a varactor diode is increased, the width Wd of the depletion layer increases. Therefore, the total junction capacitance C_T of the junction decreases.

➢ On the other hand, if the reverse voltage across the diode is lowered, the width Wd of the depletion layer decreases. Consequently, the total junction capacitance C_T increases.

➢ It is used as **Voltage Variable Capacitor, Voltage-Controlled Tuning**

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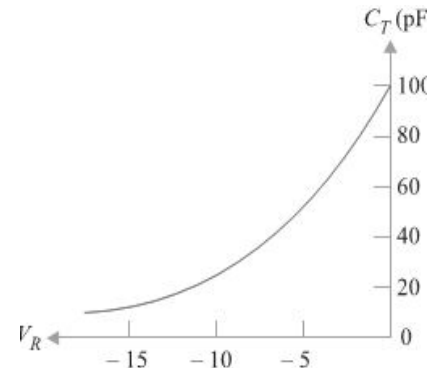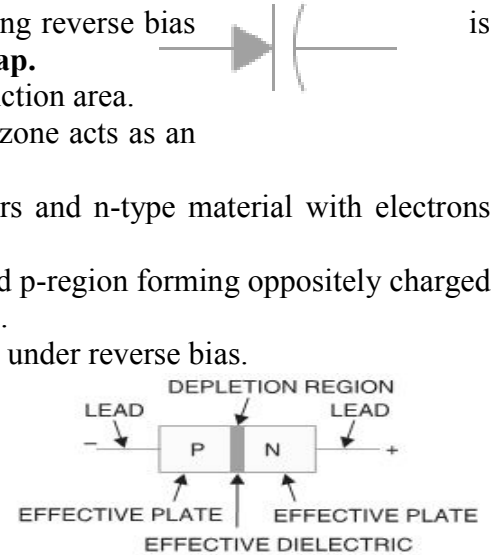
❖ INTRODUCTION: -

✍For reasons associated with economics of generation and transmission, the electric power available is usually an A.C. Supply. The supply voltage varies sinusoidal and has a frequency of 50 Hz. It is used for lighting, heating and electric motors.

✍ But there are many applications (e.g. electronic circuits) where D.C. supply is needed. When such a D.C. Supply is required, the mains A.C. Supply is rectified by using *Crystal Diodes*.

✍ The following two rectifier circuits can be used: -
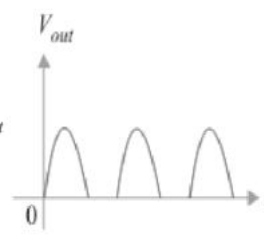 ▪ (i) Half-wave rectifier   (ii) Full-wave rectifier

✍ HALF-WAVE RECTIFIER:-

✍ In half-wave rectification, the rectifier conducts current only during the positive half-cycles of input A.C. Supply.

✍ The negative half-cycles of A.C. Supply is suppressed i.e. during negative half-cycles, no current is conducted and hence no voltage appears across the load.

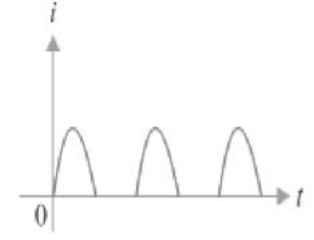✍ Therefore, current always flows in one direction through the load though after every half-cycle
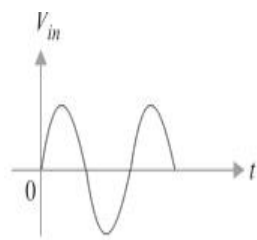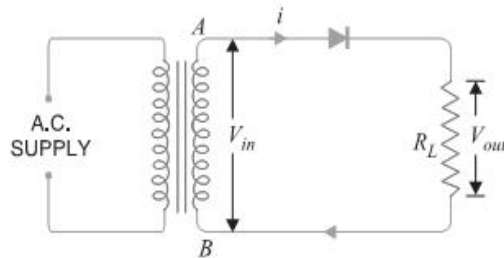
(Input Wave form)   (Half wave Rectifier Circuit)   (Output voltage wave)   (Output Current)

🞂 Circuit Details: -

🞀 The above Fig shows the circuit where a single crystal diode acts as a half-wave rectifier.

🞀 The A.C. Supply to be rectified is applied in series with the diode and load resistance R_L. Generally, A.C. Supply is given through a transformer.

🞀 The *use of transformer* permits two advantages.
- ✓ Firstly, it allows us to step up or step down the A.C. input voltage as the situation demands.
- ✓ Secondly, the transformer isolates the rectifier circuit from power line and thus reduces the risk of electric shock.

🞂 OPERATION:-

🞀 The A.C. voltage across the secondary winding AB changes polarities after every half-cycle.

🞀 During the positive half-cycle of input A.C. voltage, end A becomes positive w.r.t. end B. This makes the diode forward biased and hence it conducts current.

🞀 During the negative half-cycle, end A is negative w.r.t. end B. Under this condition, the diode is reverse biased and it conducts no current.

🞀 Therefore, current flows through the diode during positive half-cycles of input A.C. voltage only; it is blocked during the negative half-cycles. In this way, current flows through load R_L always in the same direction. Hence D.C. output is obtained across R_L.

🞀 It may be noted that output across the load is *pulsating D.C.* These pulsations in the output are further smoothened with the help of filter circuits discussed later.

🞂 Disadvantages : -

(i) The pulsating current in the load contains alternating component whose basic frequency is equal to the supply frequency. Therefore, an elaborate filtering is required to produce steady direct current.
(ii) The A.C. supply delivers power only half the time. Therefore, the output is low.

❖ FULL-WAVE RECTIFIER: -

🞀 In full-wave rectification, current flows through the load in the same direction for both half-cycles of input A.C. voltage. This can be achieved with two diodes working alternately.

🞀 For the positive half- cycle of input voltage, one diode supplies current to the load and for the negative half-cycle, the other diode does so ; current being always in the same direction through the load.

🞀 Therefore, a full-wave rectifier utilizes both half-cycles of input A.C. voltage to produce the D.C. output.

🞀 The following two circuits are commonly used for full-wave rectification: -

- ▪ **(i)** Centre-tap full-wave rectifier   **(ii)** Full-wave bridge rectifier

## ❖ CENTRE-TAP FULL-WAVE RECTIFIER:-

🞂 Circuit Details: -

🞀 The circuit employs two diodes D_1 and D_2 as shown in Fig below. A centre tapped secondary winding AB is used with two diodes connected so that each uses one half-cycle of input A.C. voltage.

🞀 In other words, diode D_1 utilizes the A.C. voltage appearing across the upper half (OA) of secondary winding for rectification while diode D_2 uses the lower half winding OB.

🞂 Circuit Operation: -

🞀 During the positive half-cycle of secondary voltage, the end A of the secondary winding becomes positive and end B negative. This makes the diode D_1 forward biased and diode D_2 reverse biased.

🞀 Therefore, diode D_1 conducts while diode D_2 does not. The conventional current flow is through diode D_1, load resistor R_L and the upper half of secondary winding as shown by the dotted arrows.

🞀 During the negative half-cycle, end A of the secondary winding becomes negative and end B positive.

- Therefore, diode D_2 conducts while diode D_1 does not. The conventional current flow is through diode D_2, load R_L & lower half winding shown by solid arrows.
- It may be seen that current in the load R_L is in the same direction for both half-cycles of input A.C. voltage. Therefore, D.C. is obtained across the load R_L.

(Input Wave form)   (Centre-Tap Full-Wave Rectifier Circuit)   (Output wave form)
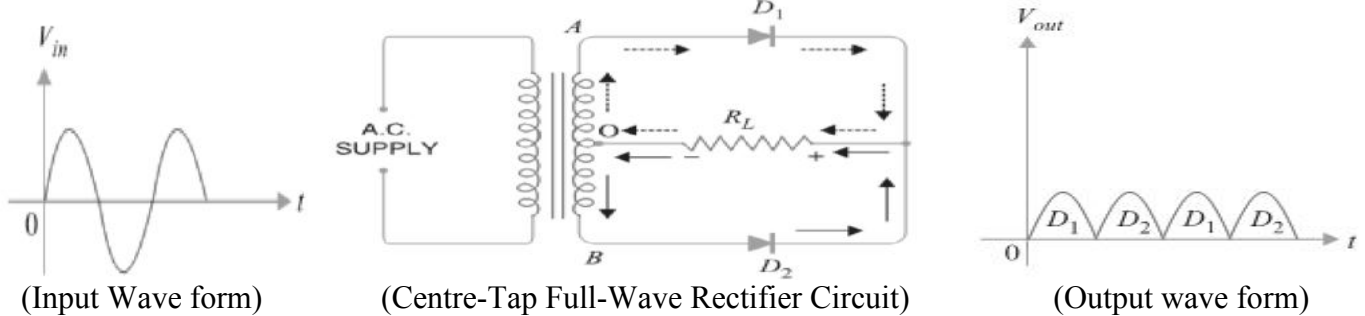
🔸 **Advantages:-**
  (i) The D.C. output voltage and load current values are twice than that of a half wave rectifier.
  (ii) The ripple factor is much less (0.482) than that of half rectifier (1.21).
 (iii) The efficiency is twice (81.2%) than that of half wave rectifier (40.6%).

🔸 **Disadvantages:-**
  (i) It is difficult to locate the centre tap on the secondary winding.
  (ii) The D.C. output is small as each diode utilizes only one-half of the transformer secondary voltage.
  (iii) The diodes used must have high peak inverse voltage.
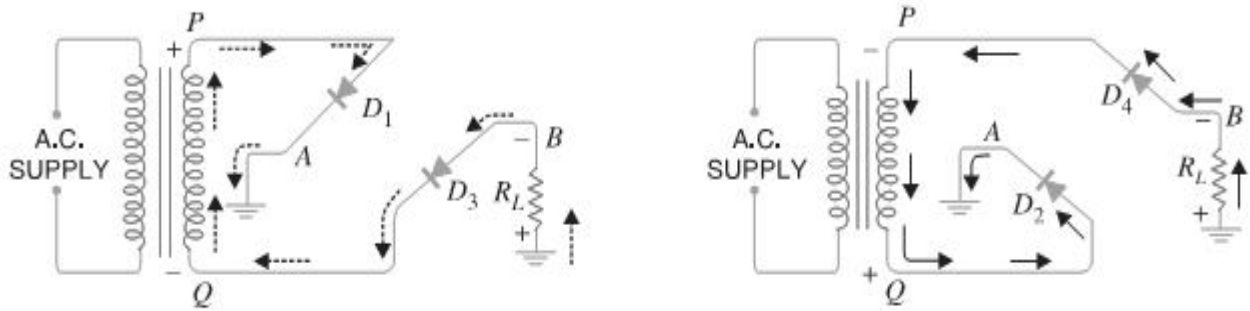
❖ **FULL-WAVE BRIDGE RECTIFIER: -**
🔸 **Circuit Details: -**
- The need for a centre tapped power transformer is eliminated in the bridge rectifier.
- It contains four diodes D_1, D_2, D_3 and D_4 connected to form bridge as shown in Fig below.
- The A.C. supply to be rectified is applied to the diagonally opposite ends of the bridge through the transformer.
- Between other two ends of the bridge, the load resistance R_L is connected.

(Input Wave Form)   (Full-Wave Bridge Rectifier Circuit)   (Output wave form)
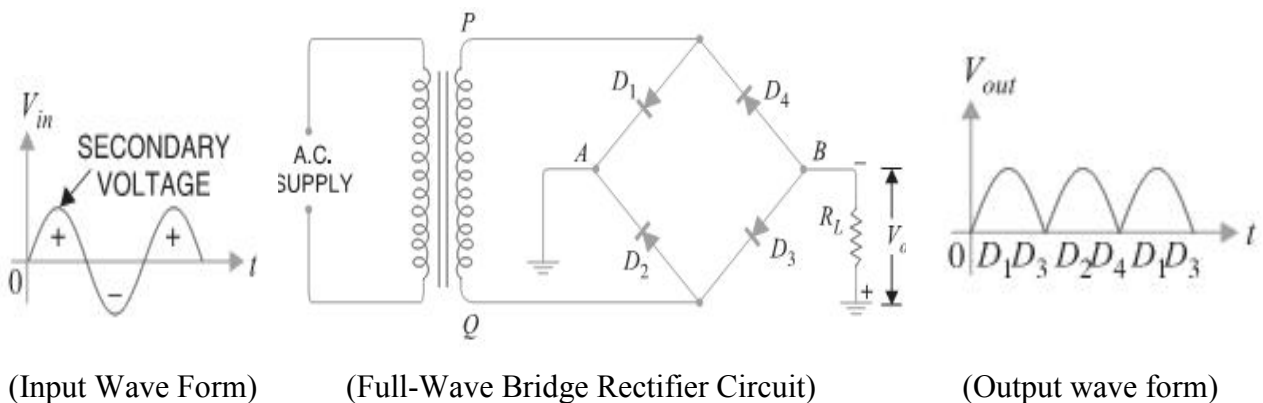
🔸 **CIRCUIT OPERATION** :-
- During the positive half-cycle of secondary voltage, the end P of the secondary winding becomes positive and end Q negative.
- This makes diodes D_1 and D_3 forward biased while diodes D2 and D4 are reverse biased.
- Therefore, only diodes D_1 and D_3 conduct. These two diodes will be in series through the load R_L as shown in Fig. below. The conventional current flow is shown by dotted arrows. It may be seen that current flows from A to B through the load R_L.
- During the negative half-cycle of secondary voltage, end P becomes negative and end Q positive. This makes diodes D_2 and D_4 forward biased whereas diodes D_1 and D_3 are reverse biased.
- Therefore, only diodes D_2 and D_4 conduct. These two diodes will be in series through the load R_L as shown in Fig. below. The current flow is shown by the solid arrows.
- It may be seen that again current flows from A to B through the load i.e. in the same direction as for the positive half-cycle. Hence, D.C. output is obtained across load R_L.

(Full-Wave Bridge Rectifier Circuit in +ve Half Cycle) (Full-Wave Bridge Rectifier Circuit -ve Half Cycle)

➢ **Advantages: -**
(i) The need for centre-tapped transformer is eliminated.
(ii) The output is twice that of the centre-tap circuit for the same secondary voltage.
(iii) The PIV is one-half that of the centre-tap circuit (for same D.C. output).

➢ **Disadvantages: -**
(i) It requires four diodes. (ii) Internal resistances high.

➕ **Mathematical Derivation for Rectification Efficiency for HALF WAVE rectifier : -**

✎ The ratio of d.c. power output to the applied input a.c. power is known as rectifier efficiency i.e.,

$$\text{Rectifier efficiency}, \eta = \frac{\text{d.c. power output}}{\text{Input a.c. power}}$$

✎ Consider a half-wave rectifier shown in Fig.

✎ Let $v = V_m \sin\theta$ be the alternating voltage that appears across the secondary winding. Let r_f and R_L be the diode resistance and load resistance respectively.

✎ The diode conducts during positive half-cycles of a.c. supply while no current conduction takes place during negative half-cycles.

❖ **OUTPUT D.C. POWER :-**

✎ The output current is pulsating direct current. Therefore, in order to find D.C. power, average current has to be found out.

$$\text{Average Value} = \frac{\text{Area Under The Curve Over a cycle}}{Base} = \int_0^\pi \frac{i\, d\theta}{2\pi}$$

$$I_{av} = I_{dc} = \frac{1}{2\pi}\int_0^\pi i\, d\theta = \frac{1}{2\pi}\int_0^\pi \frac{V_m \sin\theta}{r_f + R_L} d\theta = \frac{V_m}{2\pi(r_f + R_L)}\int_0^\pi \sin\theta\, d\theta = \frac{V_m \sin\theta}{r_f + R_L}[-\cos\theta]_0^\pi$$

$$= \frac{V_m}{2\pi(r_f + R_L)} \times [(-\cos\pi) - (-\cos 0)] = \frac{V_m}{2\pi(r_f + R_L)} \times 2 = \frac{V_m}{(r_f + R_L)} \times \frac{1}{\pi} = \frac{I_m}{\pi} \quad [\because I_m = \frac{V_m}{(r_f + R_L)}]$$

∴ D.C. Power, $\mathbf{P_{dc}} = I_{dc}^2 \times R_L = \left(\frac{I_m^2}{\pi}\right) \times R_L$

❖ **INPUT A.C. POWER**: -

✎ The A.C. power input is given by : $P_{ac} = I_{rms}^2 (r_f + R_L)$ For a half-wave rectified wave, $I_{rms} = I_m/2$

∴ $\mathbf{P_{ac}} = \left(\frac{I_m}{2}\right)^2 \times (\mathbf{r_f + R_L})$

∴ Rectifier efficiency $= \frac{\text{d.c.output power}}{\text{a.c.input power}} = \left(\frac{(I_m/\pi)^2 \times R_L}{(I_m/2)^2 (r_f + R_L)}\right) = \frac{0.406\, R_L}{r_f + R_L} = \frac{0.406 R_L}{1 + \frac{r_f}{R_L}}$

The efficiency will be maximum if r_f is negligible as compared to R_L.
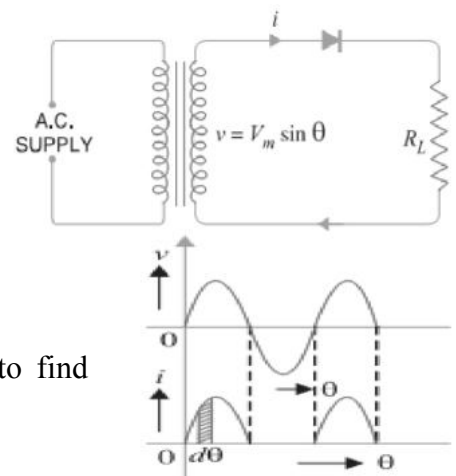
∴ **Max. Rectifier Efficiency for HALF WAVE Rectifier = 40.6%**

✎ It shows that in half-wave rectification, a maximum of 40.6% of a. c. power is converted into d. c. power.

NOTE: - $I_{rms} = [\frac{1}{2\pi}\int_0^{2\pi} i^2\, d\theta]^{1/2} = [\frac{1}{2\pi}\int_0^\pi I_m^2 \sin^2\theta\, d\theta + \frac{1}{2\pi}\int_\pi^{2\pi} 0\, d\theta]^{1/2} = [\frac{I_m^2}{2\pi}\int_0^\pi \frac{1-\cos 2\theta}{2} d\theta]^{1/2}$

$$= [\frac{I_m^2}{4\pi}[\theta - \frac{\sin 2\theta}{2}]_0^\pi]^{1/2} = [\frac{I_m^2}{4\pi}[\pi - 0 - \frac{\sin 2\pi}{2} + \sin 0]]^{1/2} = [\frac{I_m^2}{4\pi} \times \pi]^{1/2} = [\frac{I_m^2}{4}]^{1/2} = \frac{I_m}{2} \Rightarrow I_{rms} = \frac{I_m}{2}$$

Similarlly, $\mathbf{V_{rms} = V_m/2}$ for Half Wave and For Full Wave Rectifier $\mathbf{I_{rms} = I_m/\sqrt{2}}$ and $\mathbf{V_{rms} = V_m/\sqrt{2}}$

♦ Mathematical Derivation for Rectification Efficiency for FULL WAVE Rectifier : -

✎ Fig. shows the process of full-wave rectification.

✎ Let $v = V_m \sin\theta$ be the a.c. voltage to be rectified. Let rf and R_L be the diode resistance and load resistance respectively.

✎ Obviously, the rectifier will conduct current through the load in the same direction for both half-cycles of input a.c. voltage. The instantaneous current *i* is given by :

$$i = \frac{v}{(rf + R_L)} = \frac{V_m \sin\theta}{(rf + R_L)}$$
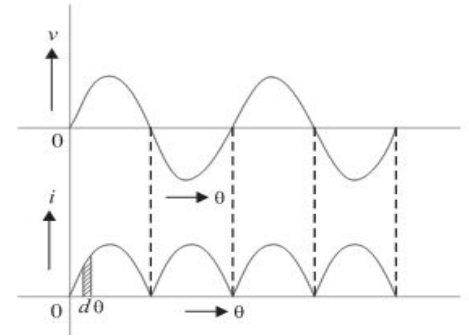
❖ D.C. OUTPUT POWER.

✎ The output current is pulsating direct current. Therefore, in order to find the d.c. power, average current has to be found out. For a full wave rectifier the average value or dc value can be found like half wave ,

$$\mathbf{I_{dc}} = \frac{2I_m}{\pi}$$

∴ D.C. power output, $\mathbf{P_{dc}} = I_{dc}^2 \times R_L = (\frac{2I_m}{\pi})^2 \times \mathbf{R_L}$

❖ A.C. INPUT POWER.

✎ The a.c. input power is given by :

$$P_{ac} = I_{rms}^2 (rf + R_L)$$

For a full-wave rectified wave, we have, $\mathbf{I_{rms}} = \mathbf{I_m}/\sqrt{2}$

∴ $\mathbf{P_{ac}} = (\frac{I_m}{\sqrt{2}})^2 (\mathbf{rf} + \mathbf{R_L})$

∴ Full-wave rectification efficiency is

$$\eta = \frac{P_{dc}}{P_{ac}} = \frac{(2I_m/\pi)^2 R_L}{(\frac{I_m}{\sqrt{2}})^2 (rf + R_L)} = \frac{8}{\pi^2} \times \frac{R_L}{(rf + R_L)} = \frac{0.812\, R_L}{rf + R_L} = \frac{0.812}{1 + \frac{rf}{R_L}}$$

The efficiency will be maximum if r_f is negligible as compared to R_L.

∴ Maximum efficiency = 81.2%

✎ This is double the efficiency due to half-wave rectifier. Therefore, a full-wave rectifier is twice as effective as a half-wave rectifier.

♦ RIPPLE FACTOR: -

✎ The output of a rectifier consists of a d.c. component and an a.c. component (also known as ripple).

✎ The a.c. component is undesirable and accounts for the pulsations in the rectifier output.

✎ The effectiveness of a rectifier depends upon the magnitude of a.c. component in the output; the smaller this component, the more effective is the rectifier.

✎ Ripple mean unwanted ac signal present in the rectified output.

✎ The ratio of R.M.S. value of A.C. component to the D.C. component in the rectifier output is known as *ripple factor* i.e.

$$\text{Ripple factor} = \frac{\text{r.m.s. value of a.c component}}{\text{value of d.c. component}} = \frac{I_{ac}}{I_{dc}}$$
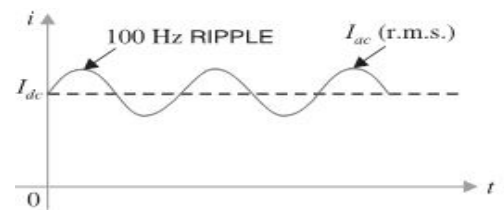
❖ Mathematical Analysis.

✎ The output current of a rectifier contains d.c. as well as a.c. component.

✎ By definition, the effective (i.e. r.m.s.) value of total load current is given by :

$$I_{rms} = \sqrt{I_{dc}^2 + I_{ac}^2} \quad \text{Or} \quad I_{ac} = \sqrt{I_{rms}^2 - I_{dc}^2}$$

✎ Dividing throughout by I_{dc}, we get,

$$\frac{I_{ac}}{I_{dc}} = \frac{1}{I_{dc}} \sqrt{I_{rms}^2 - I_{dc}^2} \quad \text{(But } I_{ac}/I_{dc} \text{ is the ripple factor.)}$$

∴ Ripple factor $= \frac{1}{I_{dc}} \sqrt{I_{rms}^2 - I_{dc}^2} = \sqrt{(\frac{I_{rms}}{I_{dc}})^2 - 1}$

(i) **For half-wave rectification: -**

In half-wave rectification, $I_{rms} = I_m/2$; $I_{dc} = I_m/\pi$

∴ Ripple factor $= \sqrt{(\frac{I_m/2}{I_m/\pi})^2 - 1} = \mathbf{1.21}$

☛ It is clear that a.c. component exceeds the d.c. component in the output of a half-wave rectifier.

☛ This results in greater pulsations in the output.

☛ Therefore, half-wave rectifier is ineffective for conversion of a.c. into d.c.

(ii) **For full-wave rectification**: -

In full-wave rectification, $I_{rms} = \frac{I_m}{\sqrt{2}}$; $I_{dc} = \frac{2I_m}{\pi}$

∴ Ripple factor $= \sqrt{(\frac{I_m/\sqrt{2}}{2I_m/\pi})^2 - 1} = \mathbf{0.48}$ i.e. $\frac{\text{effective a.c.component}}{\text{d.c.component}} = 0.48$

☛ This shows that in the output of a full-wave rectifier, the d.c. component is more than the a.c. component. Consequently, the pulsations in the output will be less than in half-wave rectifier.

☛ For this reason, full-wave rectification is invariably used for conversion of a.c. into d.c.

✚ **Peak Inverse Voltage (PIV) : -**

☛ The maximum value of reverse voltage occurs at the peak of the input cycle, which is equal to V_m.

☛ This maximum reverse voltage is called peak inverse voltage (PIV). Thus the PIV of diode : -

a) For Half Wave = V_m, **b)** For Center Tapped = $2V_m$ and **c)** For Bridge Rectifier = V_m **.**

✚ **Transformer Utilization Factor (TUF) : -**

☛ It may be defined as the ratio of d.c. power delivered to the load and the a.c. rating of the transformer secondary.

Thus, $\boxed{\mathbf{TUF = P_{dc} / P_{ac}}}$

☛ For half wave rectifier, TUF = **0.287**; Center taped rectifier, TUF = **0.693**; Bridge rectifier, TUF = **0.812**.

☛ The TUF is very useful in determining the rating of a transformer to be used with rectifier circuit.

✚ **Average Value of Voltage & Current for HALF WAVE Rectifiers: -**

☛ If V_m= Maximum value of the a.c. input voltage, then the average or d.c. value of the output voltage and current is given by

$$\boxed{\mathbf{V_{dc} = V_m/\pi = 0.318\ V_m \quad and \quad I_{dc} = I_m/\pi = 0.318\ I_m}}$$

✚ **Average Value of Voltage & Current for FULL WAVE Rectifiers: -**

☛ If V_m= Maximum value of the a.c. input voltage, then the average or d.c. value of the output voltage and current is given by

$$\boxed{\mathbf{V_{dc} = 2V_m/\pi = 0.636\ V_m \quad and \quad I_{dc} = 2I_m/\pi = 0.636\ I_m}}$$

✚ **Output Frequency of Half Wave Rectifier: -**

☛ The output frequency of a half-wave rectifier is equal to the input frequency (50 Hz). Recall how a complete cycle is defined.

☛ A waveform has a complete cycle when it repeats the same wave pattern over a given time.

☛ Thus in Fig. (i), the a.c. input voltage repeats the same wave pattern over 0° – 360°, 360° – 720° and so on.

☛ In Fig. (ii), the output waveform also repeats the same wave pattern over 0° – 360°, 360° – 720° and so on.

☛ This means that when input a.c. completes one cycle, the output half wave rectified wave also completes one cycle.

☛ In other words, for the half wave rectifier the output frequency is equal to the input frequency i.e. $\mathbf{f_{out} = f_{in}}$

☛ For example, if the input frequency of sine wave applied to a half-wave rectifier is 100 Hz, then frequency of the output wave will also be 100 Hz**.**
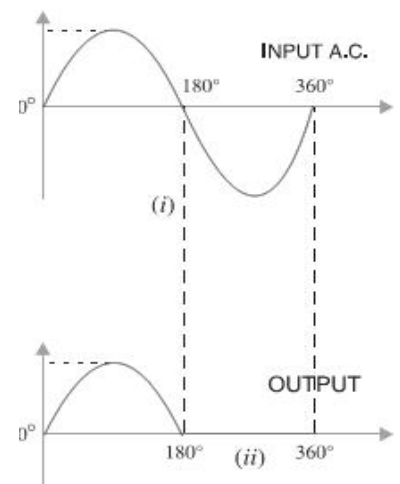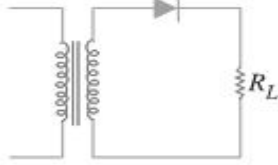
🔸 **Output Frequency of Full Wave Rectifier: -**

✎ The output frequency of a full-wave rectifier is double the input frequency.

✎ As a wave has a complete cycle when it repeats the same pattern.

✎ In Fig. (i), the input a.c. completes one cycle from 0° – 360°.

✎ However, in Fig. (ii) full-wave rectified wave completes two cycles in this period.

✎ Therefore, output frequency is twice the input frequency i.e. **$f_{out} = 2f_{in}$**

✎ For example, if the input frequency to a full-wave rectifier is 100 Hz, then the output frequency will be 200 Hz.
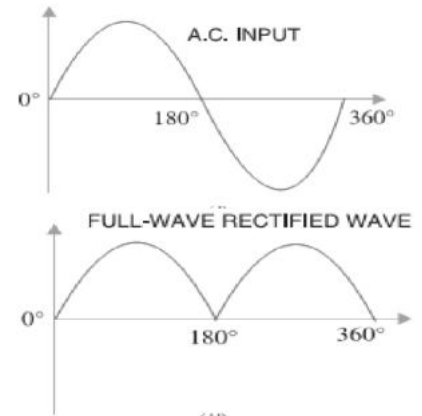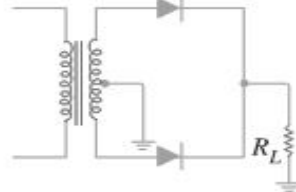
➢ **COMPARISON OF RECTIFIERS: -**
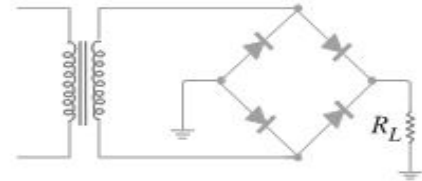
S. No.	Particulars	Half-wave	Centre-tap	Bridge type
1	No. of diodes	1	2	4
2	Transformer necessary	no	yes	no
3	Max. efficiency	40.6%	81.2%	81.2%
4	Ripple factor	1.21	0.48	0.48
5	Output frequency	f_{in}	$2f_{in}$	$2f_{in}$
6	Peak inverse voltage	V_m	$2V_m$	V_m

❖ **FILTER CIRCUITS:-**

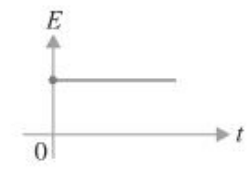✎ Generally, a rectifier is required to produce pure D.C. supply for using at various places in the electronic circuits.

✎ However, the output of a rectifier has pulsating character i.e. it contains A.C. and D.C. components.

✎ The A.C. component is undesirable and must be kept away from the load.

✎ To do so, a filter circuit is used which removes (or filters out) the A.C. component and allows only the D.C. component to reach the load.

✎ A **filter circuit** is a device which removes the A.C. component of rectifier output but allows the D.C. component to reach the load.

✎ A filter circuit is generally a combination of inductors (L) and capacitors (C).

✎ The filtering action of L and C depends upon the basic electrical principles.

✎ A capacitor offers infinite reactance to d.c.

✎ We Know that $X_C = 1/2\pi fC$. But for D.C., f = 0.

∴ $X_C = 1/2\pi fC = 1/2\pi \times 0 \times C = \infty$ (Means Capacitor shows *infinite reactance* to DC)

♣ *Hence, a Capacitor does not allow d.c. to pass through it*.

✎ We know $X_L = 2\pi fL$. For d.c., f = 0

∴ $X_L = 2\pi \times 0 \times L = 0$ (Means Inductor shows *zero reactance* to DC)

♣ *Hence Inductor passes d.c. quite readily.*

✎ *A Capacitor passes A.C. but does not pass D.C. at all. On the other hand, an Inductor opposes A.C. but allows D.C. to pass through it.*

✎ It then becomes clear that suitable network of L and C can effectively remove the A.C. component, allowing the D.C. component to reach the load.
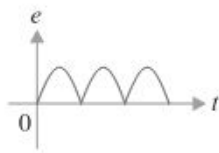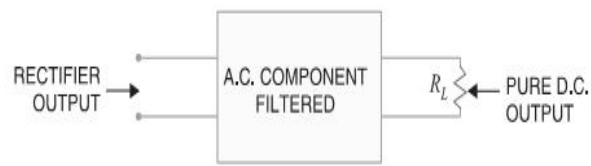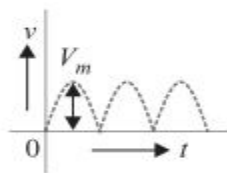
(Pulsating D.C)   (Filter Circuit)   (Pure D.C)
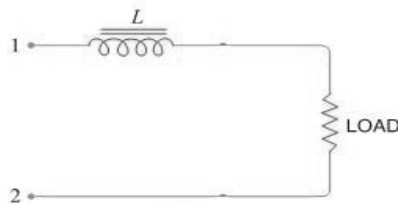
> **Types Of Filter Circuits:-**

✎ There are different types of filter circuits according to their construction. The most commonly used filter circuits are : -

   ♣ *Inductive Filter or Series Inductor,*
   ♣ *Capacitor Filter or Shunt Capacitor,*
   ♣ *Choke Input Filter or LC Filter* and
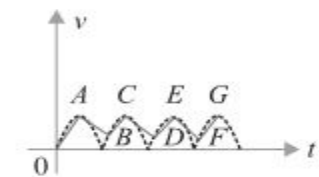   ♣ *Capacitor Input Filter* or *π-Filter*.

✓ **Inductive Filter Or Series Inductor:-**

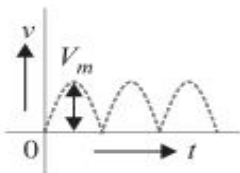(Rectified output Pulsating d.c)   (Inductive Filter Circuit)   (Output of Inductive Filter)

✎ Fig. (ii) Shows a typical Inductive filter circuit. It consists of an Inductor L placed across the rectifier output in series with load R_L.
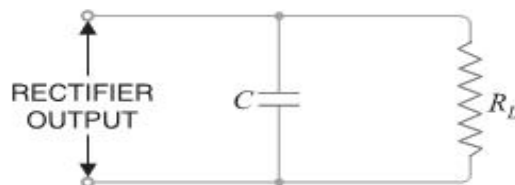
✎ The choke (Inductor with iron core) offers high opposition to the passage of a.c. component but no opposition to the d.c. component.

✎ The result is that most of the a.c. component appears across the choke while whole of d.c. component passes through the choke on its way to load. This results in the reduced pulsations at Load resistance R_L.
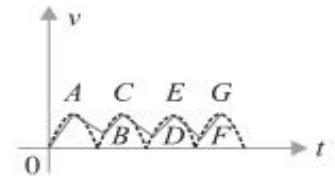
✓ **Capacitor Filter Or Shunt Capacitor:-**

(Rectified output Pulsating d.c)   (Capacitor Filter Circuit)   (Output of Capacitor Filter)

✎ Fig. (ii) Shows a typical capacitor filter circuit. It consists of a capacitor C placed across the rectifier output in parallel with load R_L.

✎ The pulsating direct voltage of the rectifier is applied across the capacitor. As the rectifier voltage increases, it charges the capacitor and also supplies current to the load.

✎ At the end of quarter cycle [Point A in Fig. (iii)], the capacitor is charged to the peak value V_m of the rectifier voltage.

✎ Now, the rectifier voltage starts to decrease. As this occurs, the capacitor discharges through the load and voltage across it decreases as shown by the line AB in Fig. (iii).

✎ The voltage across load will decrease only slightly because immediately the next voltage peak comes and recharges the capacitor.

✎ This process is repeated again and again and the output voltage waveform becomes ABCDEFG. It may be seen that very little ripple is left in the output.

✎ Moreover, output voltage is higher as it remains substantially near the peak value of rectifier output voltage.

✎ The capacitor filter circuit is extremely popular because of its low cost, small size, little weight and good characteristics.

✓ **Choke Input Filter Or LC Filter:-**
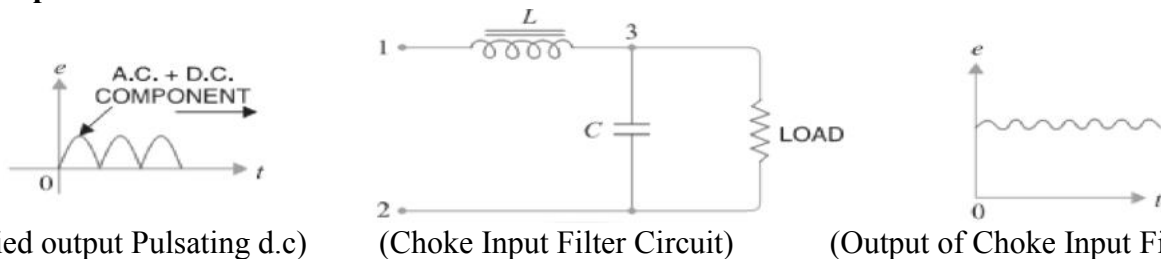
(Rectified output Pulsating d.c)   (Choke Input Filter Circuit)   (Output of Choke Input Filter)

✎ Fig. shows a typical choke input filter circuit. It consists of a choke L connected in series with the rectifier output and a filter capacitor C across the load.

✎ Only a single filter section is shown, but several identical sections are often used to reduce the pulsations as effectively as possible.

✎ The pulsating output of the rectifier is applied across terminals 1 and 2 of the filter circuit.

✎ As discussed before, the pulsating output of rectifier contains a.c. and d.c. components. The choke offers high opposition to the passage of a.c. component but negligible opposition to the d.c. component.

✎ The result is that most of the a.c. component appears across the choke while whole of d.c. component passes through the choke on its way to load. This results in the reduced pulsations at terminal 3.

✎ At terminal 3, the rectifier output contains d.c. component and the remaining part of a.c. component which has managed to pass through the choke.

✎ Now, the low reactance of filter capacitor bypasses the a.c. component but prevents the d.c. component to flow through it. Therefore, only d.c. component reaches the load.

✎ In this way, the filter circuit has filtered out the a.c. component from the rectifier output, allowing d.c. component to reach the load.

✓ **Capacitor Input Filter or π-Filter:-**
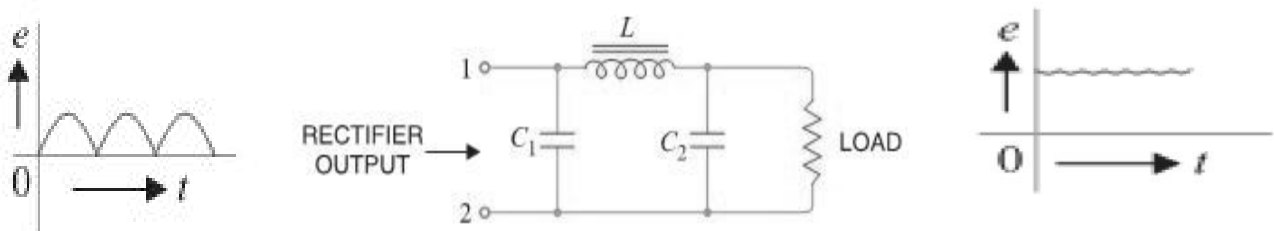
(Rectified output Pulsating d.c)   (Capacitor Input or π- Filter Circuit)   (Output of π-Filter)

✎ Fig. shows a typical capacitor input filter or π-filter. It consists of a filter capacitor C_1 connected across the rectifier output, a choke L in series and another filter capacitor C_2 connected across the load.

✎ Only one filter section is shown but several identical sections are often used to improve the smoothing action. The pulsating output from the rectifier is applied across the input terminals (i.e. terminals 1 & 2) of the filter.

✎ The filtering action of the three components viz C_1 , L and C_2 of this filter is described below :
(a) The **filter capacitor C_1** offers low reactance to a.c. component of rectifier output while it offers infinite reactance to the d.c. component. Therefore, capacitor C_1 bypasses an appreciable amount of a.c. component while the d.c. component continues its journey to the choke L.
(b) The **choke L** offers high reactance to the a.c. component but it offers almost zero reactance to the d.c. component. Therefore, it allows the d.c. component to flow through it, while the un bypassed a.c. component is blocked.
(c) The **filter capacitor C_2** bypasses the a.c. component which the choke has failed to block. Therefore, only d.c. component appears across the load and that is what we desire

[CHAPTER-2]

-------------------------- [TRANSISTORS AND CIRCUIT ANALYSIS] ----------------------

❖ **INTRODUCTION:-**

✎ When a third doped element is added to a crystal diode in such a way that two PN junctions are formed, the resulting device is known as a **Transistor**.

✎ This is a new type of electronics device which can able to amplify a weak signal in a fashion comparable and often superior to that realized by vacuum tubes.

✎ A transistor consists of two PN junctions formed by sandwiching either p-type or n-type semiconductor between a pair of opposite types. Hence Transistor is classified into two types, namely: -

   ▪ **(i)** n-p-n transistor **(ii)** p-n-p transistor

✎ An n-p-n transistor is composed of two n-type semiconductors separated by a thin section of p-type.

✎ However, a p-n-p transistor is formed by two p-sections separated by a thin section of n-type as shown in Figure below.
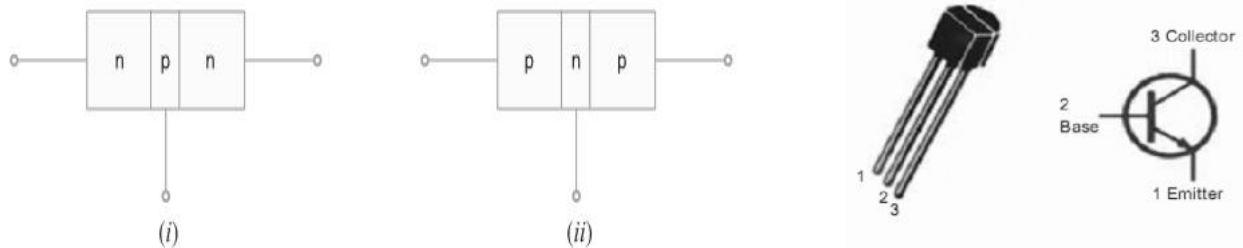

❖ **NAMING: -**

✎ A transistor has *two pn junctions*. As discussed later, one junction is forward biased and the other is reverse biased.

✎ The *forward biased junction* has a low resistance path whereas a *reverse biased junction* has a high resistance path.

✎ The weak signal is introduced in the low resistance circuit and output is taken from the high resistance circuit. Therefore, a transistor transfers a signal from a low resistance to high resistance.

✎ The prefix '**trans**' means the signal transfer property of the device while '**istor**' classifies it as a solid element in the same general family with resistors.

❖ **NAMING THE TRANSISTOR TERMINALS:-**

✎ A transistor (PNP or NPN) has three sections of doped semiconductors.

✎ The section on one side is the **emitter** and the section on the opposite side is the **collector**.

✎ The middle section is called the **base** and forms two junctions between the emitter and collector.

➕ **(i)Emitter: -**

✎ The section on one side that *supplies charge carriers* (electrons or holes) is called the emitter.

✎ The emitter is always forward biased w.r.t. base so that it can supply a large number of majority carriers.

✎ The emitter (p-type) of PNP transistor is forward biased and supplies hole charges to its junction with the base. Similarly the emitter (n-type) of NPN transistor has a forward bias and supplies free electrons to its junction with the base.

➕ **(ii) Collector: -**

✎ The section on the other side that *collects the charges* is called the collector. The collector is always reverse biased. Its function is to remove charges from its junction with the base.

✎ The collector (p-type) of PNP transistor has a reverse bias and receives hole charges that flow in the output circuit. Similarly the collector (n-type) of NPN transistor has reverse bias & receives electrons.

➕ **(iii)Base: -**

✎ The middle section which forms two PN-junctions between emitter & collector is called base.

✎ The base-emitter junction is forward biased, allowing low resistance for the emitter circuit.

✎ The base-collector junction is reverse biased and provides high resistance in the collector circuit.

(i)

(ii)
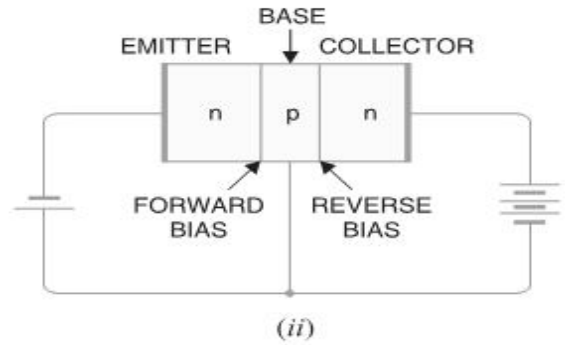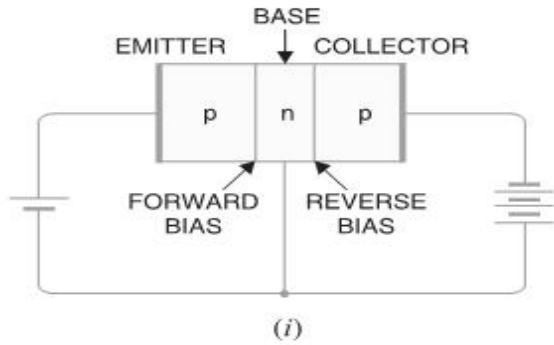
❖ **TRANSISTOR SYMBOL:-**

(i)

(ii)
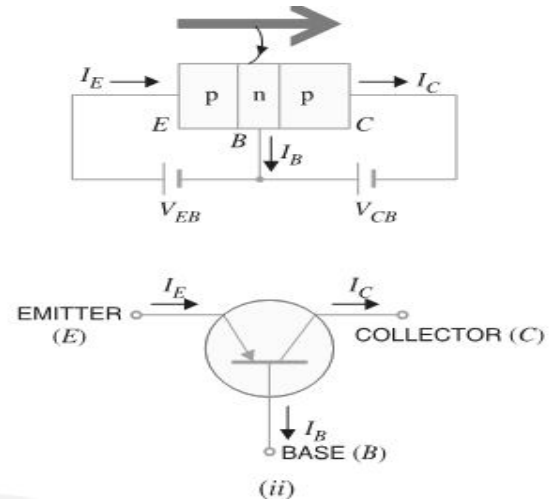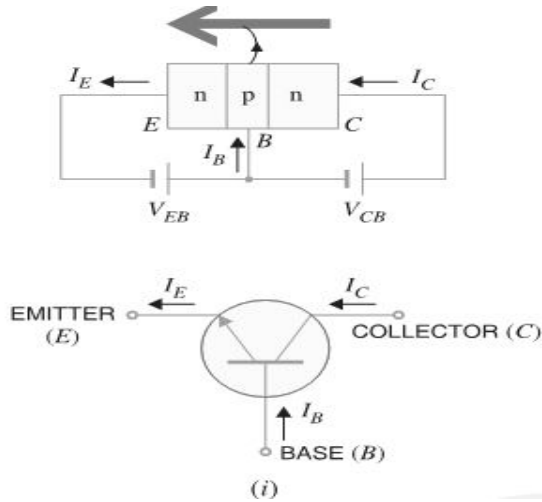
❖ **WORKING OF NPN TRANSISTOR (NPN): -**

✎ The NPN transistor with forward bias to emitter- base junction & reverse bias to collector-base junction.

✎ The forward bias causes the electrons in the n-type emitter to flow towards the base.

✎ This constitutes the emitter current I_E. As these electrons flow through the p-type base, they tend to combine with holes.

✎ As the base is lightly doped and very thin, therefore, only a few electrons (less than 5%) combine with holes to constitute base current I_B.

✎ The remainders (more than 95%) cross over into the collector region to constitute collector current I_C.

✎ In this way, almost the entire emitter current flows in the collector circuit.

✎ It is clear that emitter current is the sum of collector and base currents i.e. $I_E = I_B + I_C$
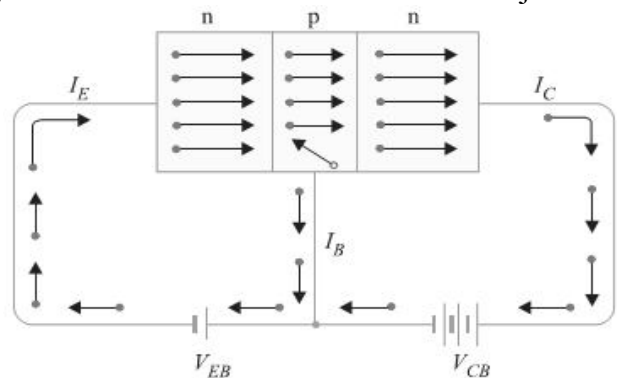
❖ **WORKING OF PNP TRANSISTOR (PNP): -**

✎ Fig. shows the basic connection of a PNP transistor.

✎ The forward bias causes the holes in the p-type emitter to flow towards the base.

✎ This constitutes the emitter current I_E.

✎ As these holes cross into n-type base, they tend to combine with the electrons.

✎ As the base is lightly doped and very thin, therefore, only a few holes (less than 5%) combine with the electrons. The remainder (more than 95%) cross into the collector region to constitute collector current I_C.

✎ In this way, almost the entire emitter current flows in the collector circuit.

✎ It may be noted that current conduction within PNP transistor is by holes. However, in the external connecting wires, the current is still by electrons
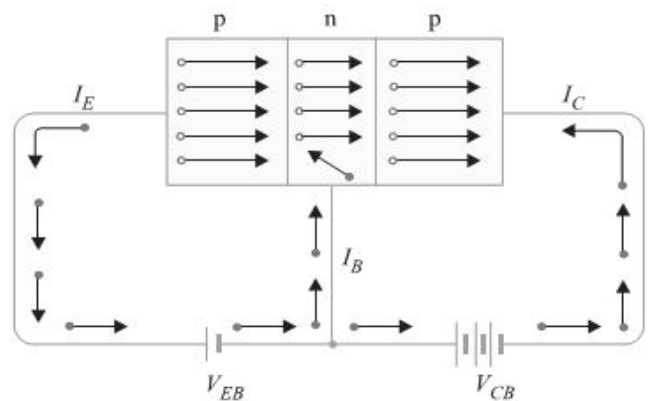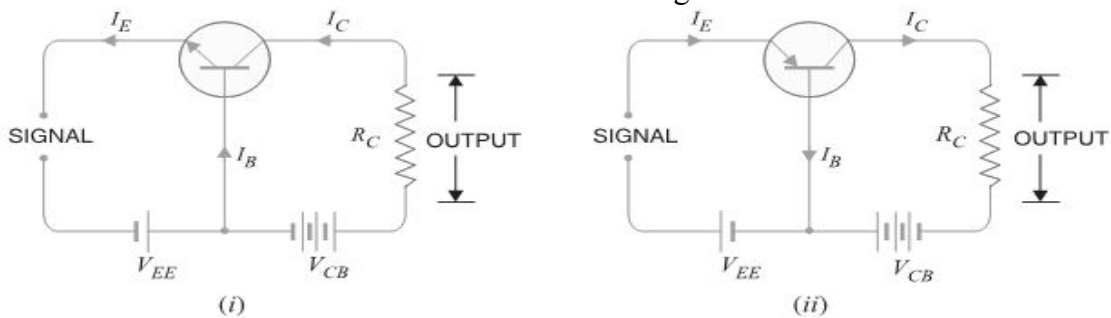
❖ TRANSISTOR CONNECTIONS:-

🔖 There are three leads in a transistor such as emitter, base and collector terminals.

🔖 However, when a transistor is to be connected in a circuit, we require **four terminals**; two for the input and two for the output.

🔖 This difficulty is overcome by making one terminal of it in common to both input and output terminals.

🔖 The input is fed between this common terminal and one of the other two terminals.

🔖 The output is obtained between the common terminal and the remaining terminal.

🔖 So a transistor can be connected in a circuit in the following ways:-

(**i**) Common Base connection (**ii**) Common Emitter connection (**iii**) Common Collector connection

➕ (i)Common Base Connection

In this circuit arrangement, input is applied between emitter and base and output is taken from collector and base.

Here, base of the transistor is common to both input and output circuits and hence the name **C**ommon **B**ase connection. A Common Base NPN and PNP in figure below.

➕ (ii) Common Emitter Connection

In this circuit arrangement, input is applied between base and emitter and output is taken from the collector and emitter.

Here, emitter of the transistor is common to both input and output circuits and hence the name **C**ommon **E**mitter connection. A Common Emitter NPN and PNP transistor circuit is shown in figure below.
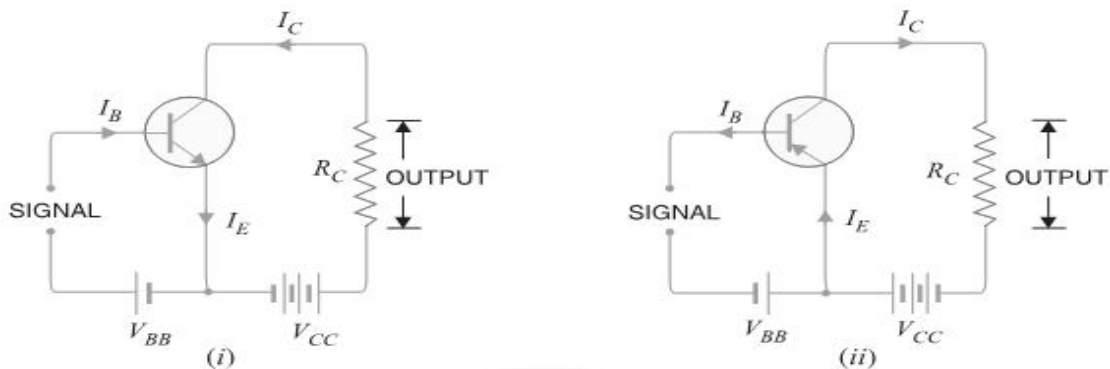
➕ (iii) Common Collector Connection

In this circuit arrangement, input is applied between base and collector while output is taken between the emitter and collector.
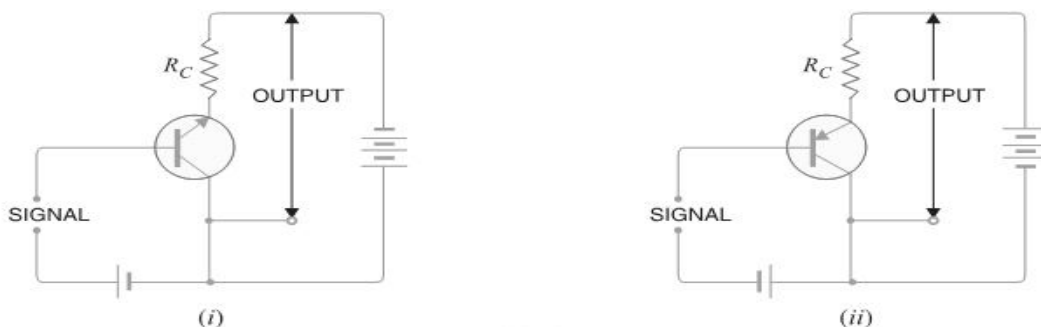
Here, collector of the transistor is common to both input and output circuits and hence the name **C**ommon **C**ollector connection. A Common Collector NPN and PNP in figure below.

❖ TRANSISTOR CHARACTERISTICS:-

⬥ 1) Characteristics of Common Base Connection

✎ The complete electrical behavior of a transistor can be described by stating the interrelation of the various currents and voltages.

✎ These relationships can be conveniently displayed graphically and the curves thus obtained are known as the characteristics of transistor.

✎ The most important characteristics of common base connection are **input characteristics** and **output characteristics**.

A) Input Characteristics:-

✎ It is the curve between emitter current I_E & emitter-base voltage V_{BE} at constant collector-base voltage V_{CB}.

✎ The emitter current is generally taken along y-axis and emitter-base voltage along x-axis. Fig. Shows the input characteristics of a typical transistor in CB arrangement.

✎ The following points may be noted from these characteristics :

♣ The emitter current I_E increases rapidly with small increase in emitter-base voltage V_{EB}. It means that input resistance is very small.

♣ The emitter current is almost independent of collector-base voltage V_{CB}. This leads to the conclusion that emitter current (and hence collector current) is almost independent of collector voltage.
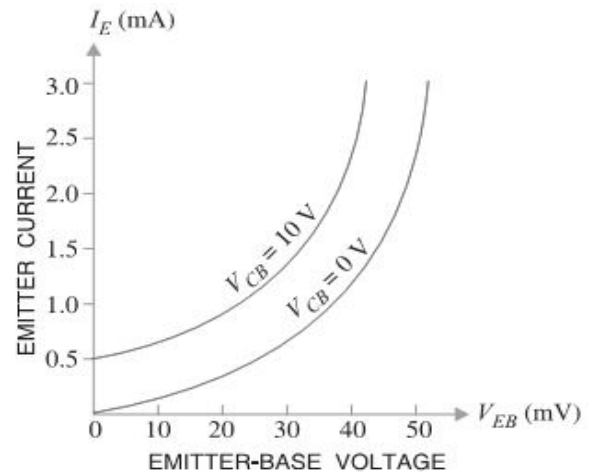
✎ **Input Resistance: -** It is the ratio of change in emitter-base voltage (ΔV_{EB}) to the resulting change in emitter current (ΔI_E) at constant collector-base voltage (V_{CB}) i.e.

$$\text{Input resistance, } r_i = \frac{\Delta V_{BE}}{\Delta I_E} \text{ at constant } V_{CB}$$

✎ In fact, input resistance is the opposition offered to the signal current. As a very small V_{EB} is sufficient to produce a large flow of emitter current I_E, thus, input resistance is quite small, of the order of a few ohms.

B) Output Characteristics:-

✎ It is the curve between collector current I_C & collector-base voltage V_{BC} at constant emitter current I_E.

✎ Generally, collector current is taken along y-axis and collector-base voltage along x-axis.

✎ The fig. shows the input and output characteristics of a typical transistor in CB arrangement.

✎ The following points may be noted from characteristics :

♣ The collector current I_C varies with V_{CB} only at very low voltages (< 1V). The transistor is never operated in this region.

♣ When the value of V_{CB} is raised above $1 - 2$ V, the collector current becomes constant as indicated by straight horizontal curves. It means that now I_C is independent of V_{CB} and depends upon I_E only. This is consistent with the theory that the emitter current flows almost entirely to the collector terminal. The transistor is always operated in this region.
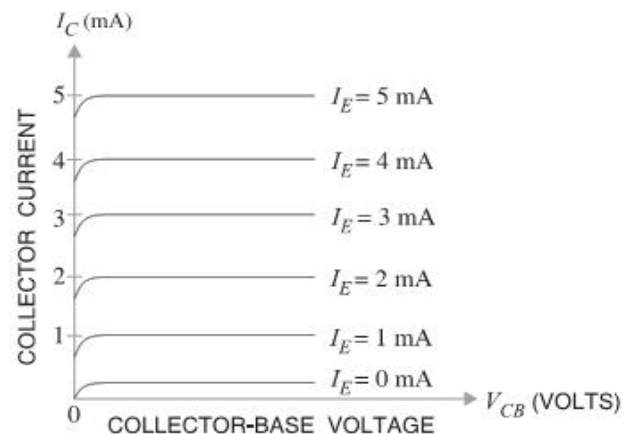
♣ A very large change in collector-base voltage produces only a tiny change in collector current. This means that output resistance is very high.

✎ **Output Resistance**: - It is the ratio of change in collector-base voltage (ΔV_{CB}) to the resulting change in collector current (ΔI_C) at constant emitter current i.e.

$$\text{Output resistance, } r_o = \frac{\Delta V_{CB}}{\Delta I_C} \text{ at constant } I_E$$

✎ The output resistance of CB circuit is very high, of the order of several tens of kilo-ohms.

➕ **2) Characteristics of Common Emitter Connection:-**

➤ The important characteristics of this circuit arrangement are the input characteristic and output characteristic.
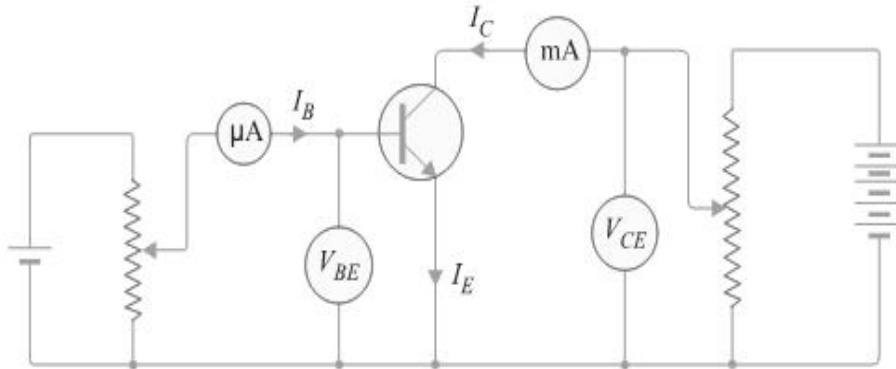
(Circuit Arrangement for studying Common Emitter Connection of Transistor)

A) **Input Characteristics:-**

✎ It is the curve between base current IB & base-emitter voltage VBE at constant collector-emitter volt V_{CE}. The input characteristics of a CE connection can be determined by the circuit shown in Fig. Keeping V_{CE} constant (Let 10 V), note the base current I_B for various values of V_{BE}.

✎ Then plot the readings obtained on the graph, taking I_B along y-axis and V_{BE} along x-axis. This gives the input characteristic at V_{CE} = 10V as shown in Fig.

✎ The following points may be noted from the characteristics :

♣ The characteristic resembles that of a forward biased diode curve. This is expected since the base-emitter section of transistor is a diode and it is forward biased.

♣ As compared to CB arrangement, I_B increases less rapidly with V_{BE}. Therefore, input resistance of a CE circuit is higher than that of CB circuit.

✎ **Input Resistance:** - It is the ratio of change in base-emitter voltage (ΔV_{BE}) to the change in base current (ΔI_B) at constant V_{CE}. The value of input resistance for CE circuit is of the order of a few hundred ohms
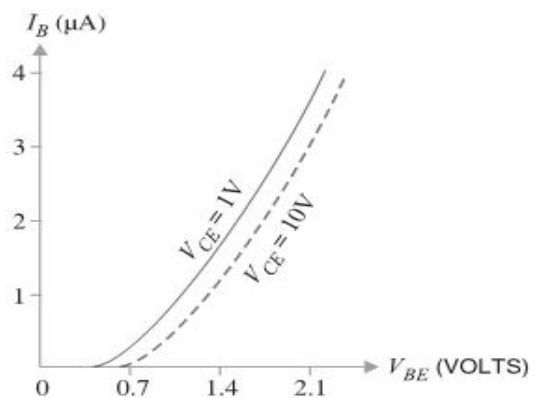
B) **Output Characteristics: -**

✎ It is the curve between collector current **I_C** and collector-emitter voltage **V_{CE}** at constant base current **I_B**.

✎ The output characteristics of CE circuit can be drawn with the help of above circuit arrangement in Fig.

✎ Keeping the base current I_B fixed at some value say, 5 μA, note the collector current I_C for various values of V_{CE}.

✎ Then plot the readings on a graph, taking I_C along y-axis and V_{CE} along x-axis.

✎ This gives the output characteristic at I_B = 5 μA as shown in Fig. The test can be repeated for I_B= 10 μA to obtain the new output characteristic as shown in Fig.

✎ Following similar procedure, a family of output characteristics can be drawn as shown in Fig.

✎ The following points may be noted from the characteristics:

♣ (i) The collector current I_C varies with V_{CE} for V_{CE} between 0 and 1V only. After this, I_C becomes almost constant & independent of V_{CE}. This value of V_{CE} upto which I_C changes with V_{CE} is called the knee voltage (V_{knee}). The transistors are always operated in the region above knee voltage.

♣ (ii) Above knee voltage, I_C is almost constant. However, a small increase in I_C with increasing V_{CE} is caused by the collector depletion layer getting wider and capturing a few more majority carriers before electron-hole combinations occur in the base area.

♣ (iii) For any value of V_{CE} above knee voltage, the collector current I_C is approximately equal to $\beta \times I_B$

➤ **Output Resistance:** - It is the ratio of change in collector-emitter voltage (ΔV_{CE}) to the change in collector current (ΔI_C) at constant I_B i.e.
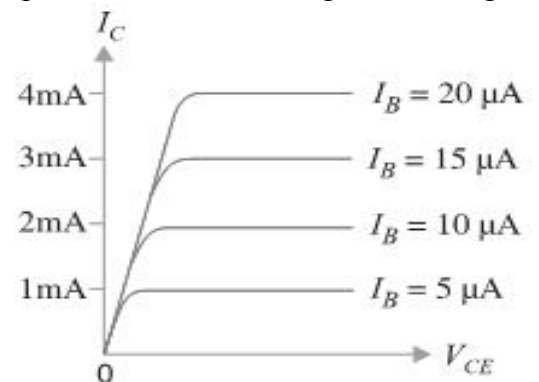
$$\text{Output resistance, } r_o = \frac{\Delta V_{CE}}{\Delta I_C} \text{ at constant } I_B$$

➢ It may be noted that whereas the output characteristics of CB circuit are horizontal, they have noticeable slope for the CE circuit.

➢ Therefore, output resistance of CE circuit is less than that of CB circuit. Its value is of the order of 50 kΩ.

3) Characteristics of Common Collector Connection:-

✎ In a Common Collector circuit connection the load resistor connected from emitter to ground, so the collector tied to ground even though the transistor is connected in a manner similar to the CE connection.

✎ Hence there is no need for a set of common-collector characteristic to choose the parameters of the circuit. The output characteristic of the CC configuration is same as CE configuration.

✎ For CC Connection the output characteristic are plot of I_E versus V_{CE} for a constant value of I_B.

✎ There is an almost unnoticeable change in the vertical scale of I_C of the CE connection if I_C is replaced by I_E for CC connection. The input circuit of CC connection, the CE characteristic is sufficient to obtain the required information.

✎ Hence Common Collector circuit connection is known as **Emitter Follower**.

❖ <u>**CURRENT AMPLIFICATION FACTORS:**</u> - (It is the ratio of output current to input current)

1) Common Base Connection:-

In a common base connection, the input current is the Emitter Current I_E and output current is the Collector Current I_C.

Hence the ratio of change in collector current to the change in emitter current at constant collector-base voltage V_{CB} is known as current amplification factor for CB Connection and is denoted as **α (Alpha).**

$$\alpha = \frac{\Delta I_C}{\Delta I_E}$$

♣ Practical values of α in commercial transistors range from 0.9 to 0.99.

2) Common Emitter Connection:-

In a common emitter connection, the input current is the Base Current I_B and output current is the Collector Current I_C.

Hence ratio of change in collector current (I_C) to the change in base current (I_B) at constant collector-emitter voltage V_{CE} is known as current amplification factor for CE Connection and denoted as **β (Beta).**

$$\beta = \frac{\Delta I_C}{\Delta I_B}$$

♣ Usually, its value ranges from 20 to 500.

3) Common Collector Connection:-

In a common collector connection, the input current is the Emitter Current I_B and output current is the Emitter Current I_E.

Hence the ratio of change in emitter current to the change in base current at constant V_{CC} is known as current amplification factor for CC Connection and is denoted as γ **(Gamma).**

$$\gamma = \frac{\Delta I_E}{\Delta I_B}$$

♣ This circuit provides about the same current gain as the common emitter circuit as $\Delta I_E \approx \Delta I_C$.

❖ **RELATION AMONG DIFFERENT CURRENT AMPLIFICATION FACTORS:-** $\boxed{\Delta I_E = \Delta I_B + \Delta I_C}$

1) Relation between α and β :-

♣ As, $\beta = \frac{\Delta I_C}{\Delta I_B} = \frac{\Delta I_C}{\Delta I_E - \Delta I_C} = \frac{\Delta I_C/\Delta I_E}{1 - \Delta I_C/\Delta I_E} = \frac{\alpha}{1-\alpha}$ ➔ As, $\alpha = \frac{\Delta I_C}{\Delta I_E} = \frac{\Delta I_C}{\Delta I_B + \Delta I_C} = \frac{\Delta I_C/\Delta I_B}{1 + \Delta I_C/\Delta I_B} = \frac{\beta}{1+\beta}$

2) Relation between α and γ :-

♣ As, $\gamma = \frac{\Delta I_E}{\Delta I_B} = \frac{\Delta I_E}{\Delta I_E - \Delta I_C} = \frac{\Delta I_E/\Delta I_E}{1 - \Delta I_C/\Delta I_E} = \frac{1}{1-\alpha}$ ➔ As, $\alpha = \frac{\Delta I_C}{\Delta I_E} = \frac{\Delta I_E - \Delta I_B}{\Delta I_E} = \frac{\Delta I_E/\Delta I_B - 1}{\Delta I_E/\Delta I_B} = \frac{\gamma - 1}{\gamma}$

3) Relation between β and γ :-

♣ As, $\gamma = \frac{\Delta I_E}{\Delta I_B} = \frac{\Delta I_B + \Delta I_C}{\Delta I_B} = \frac{\Delta I_B}{\Delta I_B} + \frac{\Delta I_C}{\Delta I_B} = 1 + \beta$ ➔ As, $\beta = \frac{\Delta I_C}{\Delta I_B} = \frac{\Delta I_E - \Delta I_B}{\Delta I_B} = \frac{\Delta I_E}{\Delta I_B} - \frac{\Delta I_B}{\Delta I_B} = \gamma - 1$

4) Relation between α, β and γ:-

♣ As, $\beta = \frac{\alpha}{1-\alpha} = \alpha \times \frac{1}{1-\alpha} = \alpha \times \gamma$ $\boxed{\therefore \beta = \alpha \times \gamma}$

$\boxed{\therefore \alpha = \frac{\beta}{1+\beta}}$ $\boxed{\therefore \beta = \frac{\alpha}{1-\alpha}}$ $\boxed{\therefore \gamma = \frac{1}{1-\alpha}}$ $\boxed{\therefore \quad _{\gamma - 1}}$ $\boxed{\therefore \gamma = 1 + \beta}$ $\boxed{\therefore \beta = \gamma + 1}$

♣ **COMPARISON OF TRANSISTOR CONNECTIONS:-**

S. No.	Characteristic	Common base	Common emitter	Common collector
1.	Input resistance	Low (about $100\ \Omega$)	Low (about $750\ \Omega$)	Very high (about $750\ k\Omega$)
2.	Output resistance	Very high (about $450\ k\Omega$)	High (about $45\ k\Omega$)	Low (about $50\ \Omega$)
3.	Voltage gain	about 150	about 500	less than 1
4.	Applications	For high frequency applications	For audio frequency applications	For impedance matching
5.	Current gain	No (less than 1)	High (β)	Appreciable

♣ Out of the three transistor connections, the **Common Emitter Circuit** is the most efficient.
♣ It is used in about 90 to 95 per cent of all transistor applications.
♣ The main reasons for the widespread use of this circuit arrangement are :
  (i) High current gain. (ii) High voltage and power gain. (iii) Moderate output to input impedance ratio.

❖ **D.C. AND A.C. EQUIVALENT CIRCUITS: -**

✎ Various circuit currents. It is useful to mention the various currents in the complete amplifier circuit. These are shown in the circuit of Fig.

✎ **(i) Base Current: -** When no signal is applied in the base circuit, D.C. base current I_B flows due to biasing circuit. When A.C. signal is applied, A.C. base current i_b also flows.

✎ Therefore, with the application of signal, Total Base Current i_B is given by: $\mathbf{i_B = I_B + i_b}$

✎ **(ii) Collector Current: -** When no signal is applied, a D.C. collector current I_C flows due to biasing circuit. When A.C. signal is applied, A.C. collector current i_c also flows.

✎ Therefore, the Total Collector Current i_C is given by: $\mathbf{i_C = I_C + i_c}$
  Where $I_C = \beta\ I_B$ = zero signal collector current and $i_c = \beta\ i_b$ = collector current due to signal.

✎ **(iii) Emitter Current:-** When no signal is applied, a D.C. emitter current I_E flows. When A.C. signal is applied, A.C. Emitter Current i_e also flows. Therefore the Total Emitter Current is : $\mathbf{i_E = I_E + i_e}$

✎ It is useful to keep in mind that: $I_E = I_B + I_C$ and $i_e = i_b + i_c$.

✎ But base current is usually very small, therefore, as a reasonable approximation, $I_E \approx I_C$ and $i_e \approx i_c$.

❖ **D. C. Equivalent Circuit: -** In order to draw the equivalent D.C. circuit, the following two steps are applied to the transistor circuit:-
  (a) Reduce all A.C. sources to zero.
  (b) Open all the capacitors.

✎ Referring D.C. Equivalent Circuit
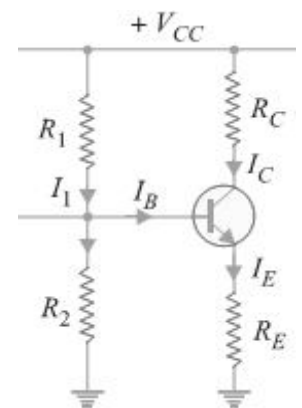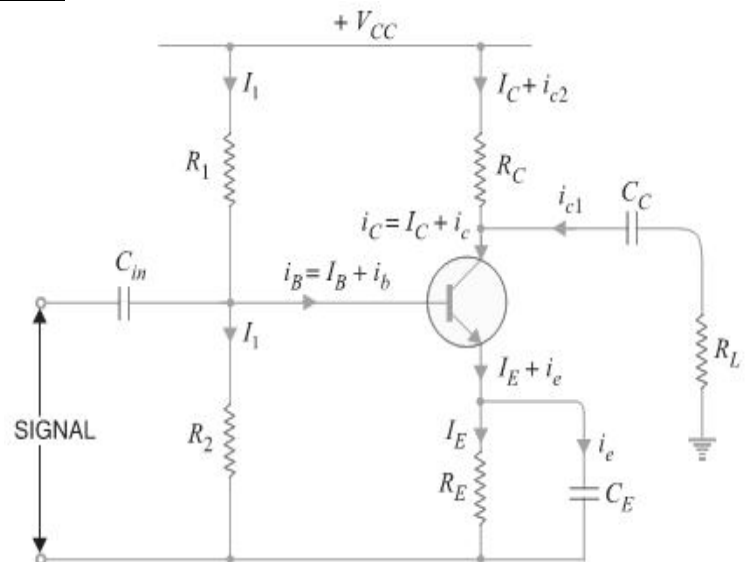 D.C. Load $\mathbf{R_{DC} = R_C + R_E}$ & $V_{CC} = V_{CE} + I_C (R_C + R_E)$

✎ The maximum value of V_{CE} will occur when there is no collector current i.e. $I_C = 0$.

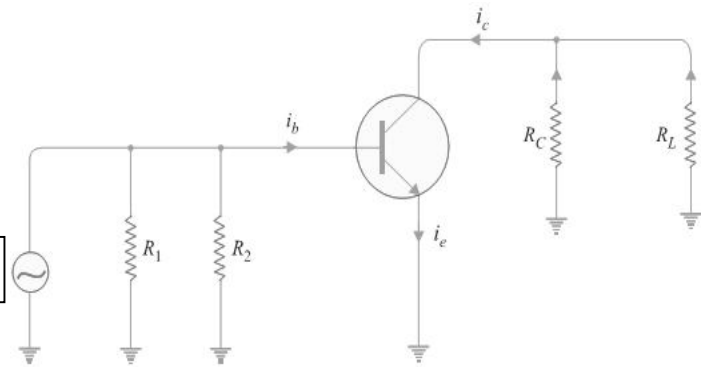 ∴ $\boxed{\textbf{Maximum } V_{CE} = V_{CC}}$

✎ The maximum collector current will flow when $V_{CE} = 0$.

  ∴ $\boxed{\textbf{Maximum } I_C = V_{CC} / (R_C + R_E)}$

❖ **A.C. Equivalent Circuit:** - In order to draw A.C. equivalent circuit, the following two steps are applied to the transistor circuit:
  (a) Reduce all D.C. sources to zero (i.e. $V_{CC} = 0$).
  (b) Short all the capacitors.

✑ Referring A.C. Equivalent circuit A.C. load equal to $R_C \parallel R_L$ i.e.

$$\boxed{\text{A.C. load, } R_{AC} = (R_C R_L / (R_C + R_L)}$$

✑ Maximum positive swing of A.C. collector-emitter voltage $= I_C \times R_{AC}$

$$\boxed{\therefore \quad \text{Total maximum \textbf{collector-emitter voltage}, } V_{CE\ MAX} = V_{CE} + I_C\ R_{AC}}$$

✑ Maximum positive swing of A.C. collector current $= V_{CE}/R_{AC}$

$$\boxed{\therefore \quad \text{Total maximum \textbf{collector current}, } I_{C\ MAX} = I_C + V_{CE}/R_{AC}}$$

❖ LOAD LINE ANALYSIS: -

✑ In the transistor circuit analysis, it is generally required to determine the collector current for various collector-emitter voltages.

✑ One of the methods can be used to plot the output characteristics and determine the collector current at any desired collector-emitter voltage. However, a more convenient method, known as **load line method** can be used to solve such problems.

✑ This method is quite easy and is frequently used in the analysis of transistor applications.
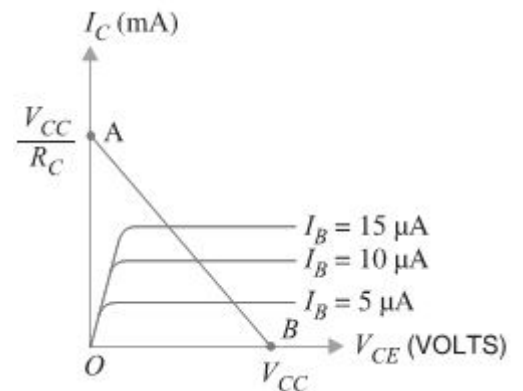
♣ **D.C. LOAD LINE**: - It is the line on the output characteristics of a transistor circuit which gives the values of I_C and V_{CE} corresponding to zero signal or D.C. conditions.

✑ Consider a common emitter NPN transistor circuit where no signal is applied. Therefore, D.C. conditions prevail in the circuit. The output characteristics of this circuit are shown in Fig.

✑ The value of collector-emitter voltage V_{CE} at any time is given by ; $\qquad V_{CE} = V_{CC} - I_C R_C \quad$ Or $\quad I_C R_C = V_{CC} - V_{CE}$
  Or $\quad I_C = V_{CC}/R_C - V_{CE}/R_C$
  Or $\quad I_C = (-1/R_C) V_{CE} + V_{CC}/R_C \quad (\equiv Y = mX + C)$

✑ As V_{CC} and R_C are fixed values, therefore, it is a first degree equation and can be represented by a straight line on the output characteristics. This is known as **D.C. Load Line.**

✑ To add load line, we need two end points of the straight line. These two points can be located as under:
  (i) When the collector current $I_C = 0$, then collector-emitter voltage is maximum and is equal to V_{CC}
  i.e. $\qquad$ Max. $V_{CE} = V_{CC} - I_C R_C = V_{CC}$ (As $I_C = 0$)

✑ This gives the first point B (OB = V_{CC}) on the collector-emitter voltage axis as shown in Fig.
  (ii) When collector-emitter voltage $V_{CE} = 0$, the collector current is maximum and is equal to V_{CC}/R_C
  i.e. $\qquad V_{CE} = V_{CC} - I_C R_C$ or $0 = V_{CC} - I_C R_C$
  $\qquad \therefore \qquad$ Max. $I_C = V_{CC}/R_C$

✑ This gives the second point A (OA = V_{CC}/R_C) on the collector current axis as shown in Fig.

✑ By joining these two points, **D.C. Load Line** AB is constructed.
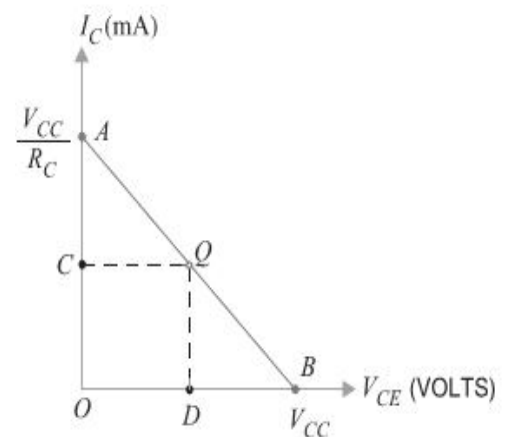
♣ **(II) A.C. LOAD LINE.** This is the line on the output characteristics of a transistor circuit which gives the values of i_C and v_{CE} when signal is applied.

✎ Referring back to the transistor amplifier shown in Fig., its A.C. equivalent circuit as far as output circuit is concerned is as shown in Fig.

✎ To add A.C. load line to the output characteristics, we again require two end points: –
1. One maximum collector-emitter voltage point **($V_{CE\ MAX}$)** and
2. Other is maximum collector current point. **($I_{C\ MAX}$)**

✎ Under the application of A.C. signal, these values are Maximum collector-emitter voltage, **$V_{CE\ MAX} = V_{CE} + I_C R_{AC}$.**

✎ This locates the point C of the A.C. load line on the collector-emitter voltage axis.

✎ Maximum collector current, **$I_{C\ MAX} = I_C + V_{CE}/R_{AC}$**

✎ This locates the point D of A.C. load line on the collector-current axis.

✎ By joining points C and D, the **A.C. Load Line** CD is constructed.
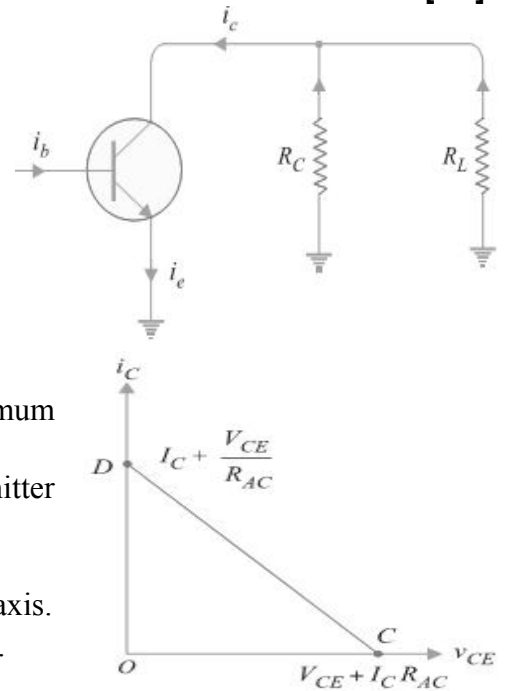
❖ OPERATING POINT: -

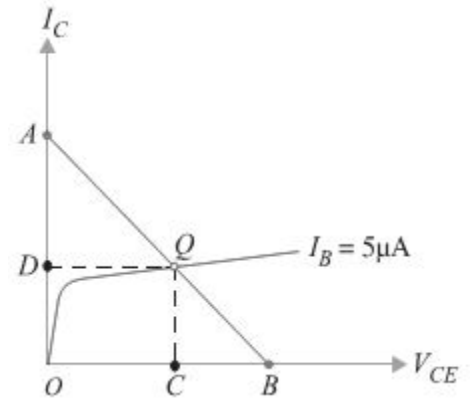✎ The zero signal values of I_C and V_{CE} are known as the **Operating point**.

✎ It is called operating point because the variations of I_C and V_{CE} take place about this point when signal is applied.

✎ It is also called quiescent (silent) point or **Q-Point** because it is the point on I_C –V_{CE} characteristic when the transistor is silent i.e. in the absence of the signal.

✎ Suppose in the absence of signal, the base current is 5µA. Then I_C and V_{CE} conditions in the circuit must be represented by some point on $I_B = 5$ µA characteristic.

✎ But I_C and V_{CE} conditions in the circuit should also be represented by some point on the d. c. load line AB.

✎ The point Q where the load line and the characteristic intersect is the only point which satisfies both these conditions. Therefore, the point Q describes the actual state of affairs in the circuit in the zero signal conditions and is called the operating point. Referring to Fig, for $I_B = 5$ µA, the zero signal values are :

$$V_{CE} = OC \text{ volts} \qquad I_C = OD \text{ mA}$$

✎ It follows, therefore, that the zero signal values of I_C and V_{CE} (i.e. operating point) are determined by the point where d.c. load line intersects at proper base current curve.

❖ THE LEAKAGE CURRENT:-

✎ The current is due to the movement of minority carriers is known as Leakage Current.

✎ In Common Base Connection of Transistor the leakage current **I_{CBO}** is the Collector-Base current with emitter open.

✎ Similarly, In Common Emitter Connection the leakage current **I_{CEO}** is the Collector-Emitter Current with open Base.

✎ Expression for collector current in Common Base Connection is given by,

$$I_C = \frac{\alpha}{1-\alpha} I_B + \frac{I_{CBO}}{1-\alpha}$$

✎ Expression for collector current in Common Emitter Connection is given by,

$$I_C = \frac{\alpha}{1-\alpha} I_B + \frac{1}{1-\alpha} I_{CBO} \quad \text{Or} \quad I_C = \frac{\alpha}{1-\alpha} I_B + I_{CEO}$$
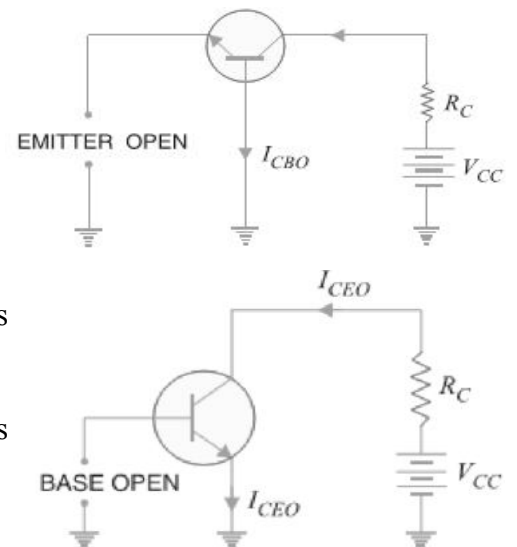
❖ FAITHFUL AMPLIFICATION :-

✎ The process of raising the strength of a weak signal without any change in its general shape is known as *Faithful Amplification*. The key factor for achieving faithful amplification: -
- ♣ (i) Proper zero signal collector current
- ♣ (ii) Minimum proper base-emitter voltage (V_{BE}) at any instant
- ♣ (iii) Minimum proper collector-emitter voltage (V_{CE}) at any instant

❖ TRANSISTOR BIASING: -

✎ The proper flow of zero signal collector current and the maintenance of proper collector-emitter voltage during the passage of signal is known as *Transistor Biasing*.

✎ The following are the most commonly used methods of obtaining transistor biasing from one source of supply (i.e. V_{CC}):
- ♣ (i) Base Resistor Method
- ♣ (ii) Emitter Bias Method
- ♣ (iii) Biasing with Collector-Feedback Resistor
- ♣ (iv) Voltage-Divider Bias.

❖ STABILISATION: -

✎ The process of making operating point independent of temperature changes or variations in transistor parameters is known as *Stabilization*.

❖ NEED FOR STABILIZATION:- Stabilization of the operating point is necessary due to the following reasons :
- ♣ (i) Temperature dependence of IC
- ♣ (ii) Individual variations
- ♣ (iii) Thermal runaway

✎ The self-destruction of an unsterilized transistor is known as ***Thermal Runaway***.

❖ STABILITY FACTOR :-

✎ The rate of change of collector current I_C w.r.t. the collector leakage current I_{CO} [= I_{CEO}] at constant β and I_B is called stability factor i.e.

$$\text{Stability factor, } S = \frac{dI_C}{dI_{CO}} \text{ at constant } I_B \text{ and } \beta$$

❖ SIMPLE PROBLEMS ON TRANSISTOR: -

1. In a common base connection, $I_E = 1mA$, $I_C = 0.95mA$. Calculate the value of I_B.

Solution: Using the relation, $I_E = I_B + I_C$

Or $1 = I_B + 0.95$ ∴ $I_B = 1 - 0.95 =$ **0.05 mA**

2. In a common base connection, current amplification factor is 0.9. If the emitter current is 1mA, determine the value of base current.

Solution: Here, $\alpha = 0.9$, $I_E = 1$ mA

Now $\alpha = \frac{I_C}{I_E}$ Or $I_C = \alpha I_E = 0.9 \times 1 = 0.9$ mA

Also $I_E = I_B + I_C$ ∴ Base current, $I_B = I_E - I_C = 1 - 0.9 =$ **0.1 mA**

3. In a common base connection, the emitter current is 1mA. If the emitter circuit is open, the collector current is 50 μA. Find the total collector current. Given that α = 0.92.

Solution: Here, $I_E = 1$ mA, α = 0.92, $I_{CBO} = 50$ μA

∴ Total collector current, $I_C = \alpha I_E + I_{CBO} = 0.92 \times 1 + 50 \times 10^{-3} = 0.92 + 0.05 =$ **0.97 mA**

4. In a common base connection, α = 0.95. The voltage drop across 2 kΩ resistance which is connected in the collector is 2V. Find the base current.

Solution: The voltage drop across R_C (= 2 kΩ) is 2V. ∴ $I_C = 2$ V/2 kΩ = 1 mA

Now $\alpha = I_C/I_E$ ∴ $I_E = \frac{I_C}{\alpha} = \frac{1}{0.95} = 1.05$ mA

Using the relation, $I_E = I_B + I_C$ ∴ $I_B = I_E - I_C = 1.05 - 1 =$ **0.05 mA**

5. For the common base circuit shown in Fig. determine I_C & V_{CB}. Assume the transistor is Silicon.

Solution: Since the transistor is of silicon, $V_{BE} = 0.7V$.

Applying Kirchhoff's voltage law to the emitter-side loop, we get,

$$V_{EE} = I_E R_E + V_{BE}$$

Or $\qquad I_E = \frac{V_{EE} - V_{BE}}{R_E} = \frac{8V - 0.7V}{1.5\ K\Omega} = 4.87$ mA

$\qquad \therefore \qquad I_C \approx I_E = \textbf{4.87 mA}$

Applying Kirchhoff's voltage law to the collector-side
loop, we have,

$$V_{CC} = I_C R_C + V_{CB} \Rightarrow V_{CB} = V_{CC} - I_C R_C =$$

18 V -4.87 mA $\times 1.2$ k$\Omega = \textbf{12.16 V}$

6. Calculate I_E in a transistor for which $\beta = 50$ and $I_B = 20\ \mu A$.

Solution: Here $\beta = 50$, $I_B = 20\mu A = 0.02$ mA

Now $\quad \beta = \frac{I_C}{I_B} \quad \therefore \quad I_C = \beta I_B = 50 \times 0.02 = 1$ mA ; Using the relation, $I_E = I_B + I_C = 0.02 + 1 = \textbf{1.02mA}$

7. For a transistor, $\beta = 45$ and voltage drop across 1kΩ which is connected in the collector circuit is 1 volt. Find the base current for common emitter connection.

Solution: Fig. shows the required common emitter connection.

The voltage drop across R_C (= 1 kΩ) is 1volt.

$\qquad \therefore \qquad I_C = \frac{1\ V}{1\ K\Omega}$

Now $\qquad \beta = \frac{I_C}{I_B} \qquad \therefore \qquad I_B = \frac{I_C}{\beta} = \frac{1}{45} = \textbf{0.022 mA}$

8. A transistor is connected in common emitter (CE) configuration in which collector supply is 8V and the voltage drop across resistance R_C connected in the collector circuit is 0.5V. The value of $R_C = 800\ \Omega$. If $\alpha = 0.96$, Determine :

(i) Collector-emitter voltage

(ii) Base current

Solution: Fig. shows the required common emitter connection with
Various values. (i) Collector-Emitter voltage,

$$V_{CE} = V_{CC} - 0.5 = 8 - 0.5 = \textbf{7.5 V}$$

(ii) The voltage drop across R_C (= 800 Ω) is 0.5 V.

$\qquad \therefore \qquad I_C = \frac{0.5\ V}{800\ \Omega} = \frac{5}{8}$ mA $= 0.625$ mA

Now $\quad \beta = \frac{\alpha}{1-\alpha} = \frac{0.96}{1-0.96} = 24 \quad \therefore$ Base current, $I_B = \frac{I_C}{\beta} = \frac{0.625}{24} = \textbf{0.026 mA}$

9. For the circuit shown in Fig. , Draw the D.C. load line.

Solution: $V_{CE} = V_{CC} - I_C R_C$, When $I_C = 0 \Rightarrow V_{CE} = V_{CC} = \textbf{12.5 V}$

This locates the point B of the load line on collector – emitter voltage axis.

When $V_{CE} = 0 \Rightarrow I_C = V_{CC} / R_C = 12.5V/2.5$ k$\Omega = \textbf{5mA}$

This locates the point A of the load line on collector current axis.

By joining these two points, we get the D.C. load line AB.

10. In the circuit diagram shown in Fig. (i), if $V_{CC} = 12V$ and $R_C = 6K\Omega$, draw the d.c. load line. What will be the Q point if zero signal base current is 20μA and $\beta = 50$?

Solution: The collector – emitter voltage V_{CE} is given by: $V_{CE} = V_{CC} - I_C R_C$

When $I_C = 0$, $V_{CE} = V_{CC} = \textbf{12V.}$ This locates the point B of the load
line. When $V_{CE} = 0$, $I_C = V_{CC}/R_C = 12V/6$ k$\Omega = \textbf{2 mA}$. This locates the
point A of Load Line. By joining these two points, load line AB is constructed.
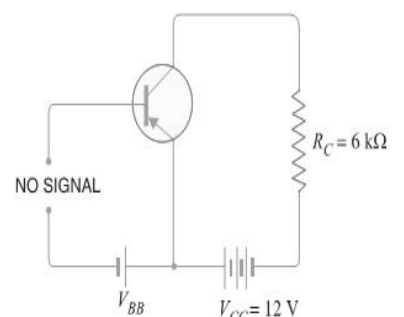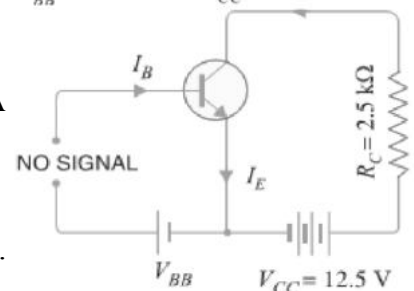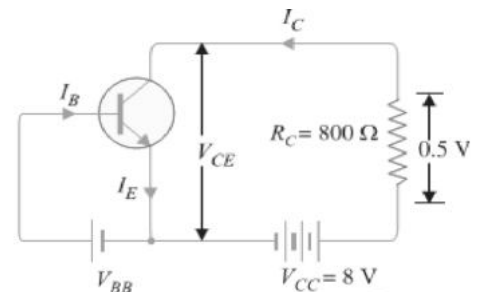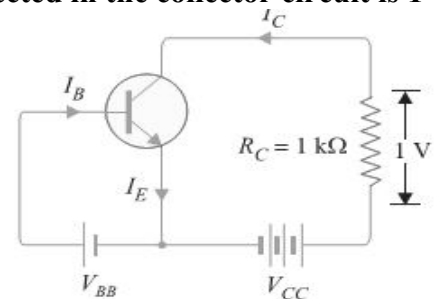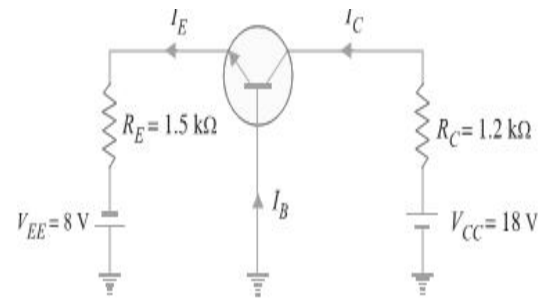
Zero signal base current, $I_B = 20\ \mu A = 0.02$ mA Current amplification factor, $\beta = 50$

∴ Zero signal collector current, $I_C = \beta I_B = 50 \times 0.02 = \mathbf{1\ mA}$

Zero signal collector – emitter voltage is $V_{CE} = V_{CC} - I_C R_C = 12 - 1mA \times 6\ k\Omega = \mathbf{6V}$.

∴ Operating point is 6V, 1mA

Fig. (ii) Shows the Q point. Its co-ordinate are $I_C = 1mA$ and $V_{CE} = 6V$.

11. Fig. Shows that a silicon transistor with β = 100 is biased by Base resistor method. Draw D.C. the Load Line & Determine Operating point.

Solution: $V_{CC} = 6V$, $R_B = 530\ k\Omega$, $R_C = 2\ k\Omega$

D.C. Load Line. Referring to Fig. (i), $V_{CE} = V_{CC} - I_C R_C$

When $I_C = 0$, $V_{CE} = V_{CC} = \mathbf{6V}$. This locates the first point B (OB = 6V) of load line on collector – emitter voltage axis as shown in Fig. (ii). When $V_{CE} = 0$, $I_C = V_{CC}/R_C = 6V/2\ k\Omega = \mathbf{3\ mA.}$

This locates the second point A (OA=3mA) of the load line on the collector current axis. By joining points A and B, D.C. Load Line AB is constructed.

Operating point Q. as it is silicon transistor, therefore, $V_{BE} = 0.7V$.

Referring to Fig. (i), it is clear that:

$$I_B R_B + V_{BE} = V_{CC}$$

Or $\quad I_B = \dfrac{V_{CC} - V_{BE}}{R_B} = \dfrac{(6 - 0.7)V}{530\ k\Omega} = 10\mu A$

∴ Collector current, $I_C = \beta I_B = 100 \times 10 = 1000\ \mu A = \mathbf{1mA}$

Collector-emitter voltage, $V_{CE} = V_{CC} - I_C R_C = 6 - 1mA \times 2\ k\Omega = 6 - 2 = \mathbf{4V}$

∴ Operating point is (4V, 1mA.) Fig. (ii) Shows the operating point Q on the D.C. load line. Its co-ordinates are $I_C = 1mA$ and $V_{CE} = 4V$.

12. *Fig. shows a silicon transistor biased by feedback resistor method. Determine the operating point. Given that β = 100.*

Solution: $V_{CC} = 20V$, $R_B = 100k\Omega$, $R_C = 1\ k\Omega$. Since it is silicon transistor, $V_{BE} = 0.7V$.

Assuming I_B to be in mA and using the relation,

$$R_B = \dfrac{V_{CC} - V_{BE} - \beta I_B R_C}{I_B} \quad Or \quad 100 \times I_B = 20 - 0.7 - 100 \times I_B \times 1 \rightarrow 200\ I_B = 19.3$$

$\rightarrow I_B = \dfrac{19.3}{200} = 0.096$ mA ∴ Collector current, $I_C = \beta I_B = 100 \times 0.096 = \mathbf{9.6\ mA}$

Again $V_{CE} = V_{CC} - I_C R_C = 20 - 9.6\ mA \times 1\ k\Omega = \mathbf{10.4\ V}$

∴ Q-Point is (10.4V, 9.6mA.)

13. Fig. shows the voltage divider bias method. Draw the D.C. Load Line and determine the operating point. Assume the transistor to be of silicon.

Solution: *D.C. Load Line.* The collector-emitter voltage V_{CE} is given by:

$\quad V_{CE} = V_{CC} - I_C (R_C + R_E)$ When $I_C = 0$, $V_{CE} = V_{CC} = \mathbf{15V.}$

♣ This locates the first point B (OB= 15V) of the load line on the collector-emitter voltage axis. When $V_{CE} = 0$, $I_C = V_{CC}/(R_C + R_E) = 15\ V/(1 + 2)\ k\Omega = \mathbf{5\ mA}$

♣ This locates the second point A (OA=5mA) of the load line on collector current axis. By joining points A & B, the D.C. Load Line AB is constructed as in Fig.

Operating Point: - For silicon Transistor, $V_{BE} = 0.7$ V

Voltage across 5 kΩ is $V_2 = [V_{CC}/(10+5)] \times 5$

Or $V_2 = (15 \times 5)/(10+5) = 5$ V

Voltage drop across $R_2 = \left(\dfrac{V_{CC}}{R_1 + R_2}\right) R_2$

∴ Emitter current, $I_E = (V_2 - V_{BE})/R_E = (5 - 0.7)/2k\Omega = 4.3/2k\Omega = 2.15$ mA

∴ Collector current is $I_C \approx I_E = \mathbf{2.15\ mA}$

Collector-Emitter volt, $V_{CE} = V_{CC} - I_C (R_C + R_E) = 15 - 2.15mA \times 3k\Omega = \mathbf{8.55V}$

∴ Operating point is (8.55 V, 2.15 mA) is shown in Fig.
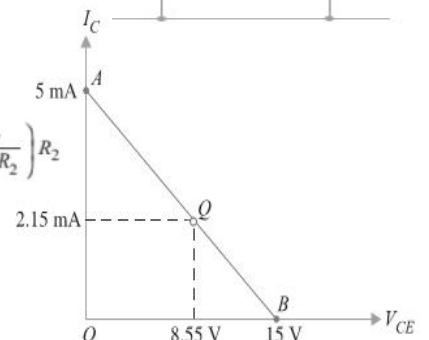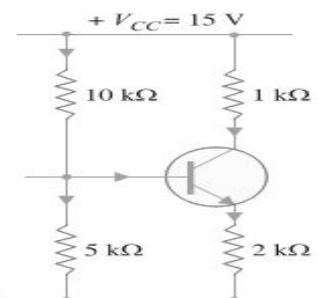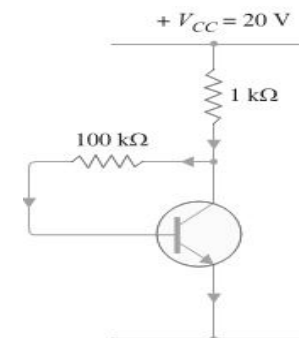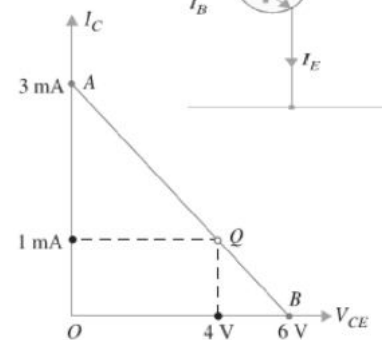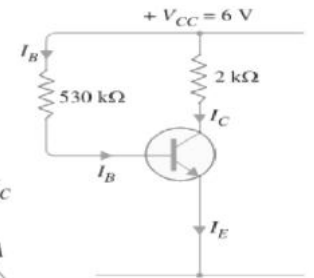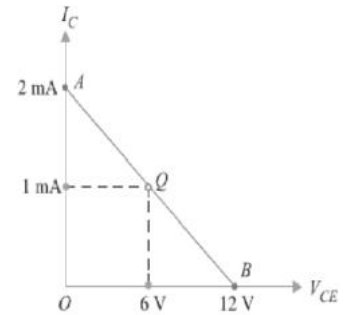
❖ **AMPLIFIER:-**

✍ The device which increases the strength of a weak signal is known as *Amplifier*. This can achieve by use of Transistor. It may be classified according to the number of stage of amplification, Such as:-
  1) Single stage transistor amplifier.
  2) Multi stage transistor amplifier.

✓ **Single Stage Transistor Amplifier: -** When only one transistor with associated circuitry is used for amplifying a weak signal, the circuit is known as *Single Stage Transistor Amplifier*.

✓ **Multi stage Transistor Amplifier:-**When a transistor circuit containing more than one stage of amplification is known as *Multi stage Transistor Amplifier*.

❖ **SINGLE STAGE TRANSISTOR AMPLIFIER:-**

✍ A single stage transistor amplifier has one transistor, bias circuit and other auxiliary components.

✍ When a weak A.C. signal is given to the base of transistor, a small base current starts flowing.

✍ Due to transistor action, a much larger (β times the base current) current flows through the collector load R_C.

✍ As the value of R_C is quite high (usually 4-10 kΩ), therefore, a large voltage appears across R_C.

✍ Thus, a weak signal applied in the base circuit appears in amplified form in the collector circuit.

✍ It is in this way that a transistor acts as an amplifier.

❖ **Graphical Demonstration of Transistor Amplifier:-**

[Transistor as an Amplifier]

✍ The function of transistor as an amplifier can also be explained graphically. The given Fig shows the output characteristics of a transistor in CE configuration.

✍ Suppose the zero signal base current is 10 µA i.e. this is the base current for which the transistor is biased by the biasing network.

✍ When an A.C. signal is applied to the base, it makes the base, say positive in the first half-cycle and negative in the second half cycle.

✍ Therefore, the base and collector currents will increase in the first half-cycle when base-emitter junction is more forward-biased.

✍ However, they will decrease in the second half-cycle when the base-emitter junction is less forward biased.

✍ For example, consider a sinusoidal signal which increases or decreases the base current by 5 µA in the two half-cycles of the signal. It is clear that in the absence of signal, the base current is 10µA and the collector current is 1 mA. However, when the signal is applied in the base circuit, the base current and hence collector current change continuously.

✍ In the first half-cycle peak of the signal, the base current increases to 15 µA and the corresponding collector current is 1.5 mA. In the second half-cycle peak, the base current is reduced to 5 µA and the corresponding collector current is 0.5 mA.

✍ For other values of the signal, the collector current is in between these values i.e. 1.5 mA and 0.5 mA. It is clear from above fig that 10 µA base current variation results in 1mA (1,000 µA) collector current variation i.e. by a factor of 100.

✍ This large change in collector current flows through collector resistance R_C. The result is that output signal is much larger than the input signal. Thus, the transistor has done amplification.

❖ **MULTI STAGE TRANSISTOR AMPLIFIER:-**

✍ The output from a single stage amplifier is usually insufficient to drive an output device. In other words, the gain of a single amplifier is inadequate for practical purposes.

✍ Consequently, additional amplification over two or three stages is necessary. To achieve this, the output of each amplifier stage is coupled in some way to the input of the next stage.

✍ The resulting system is referred to as multistage amplifier.
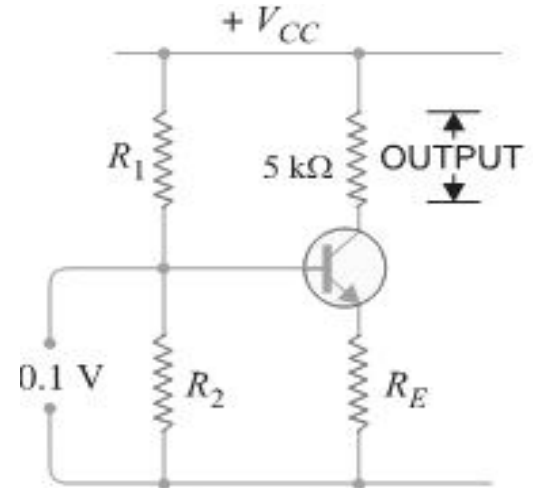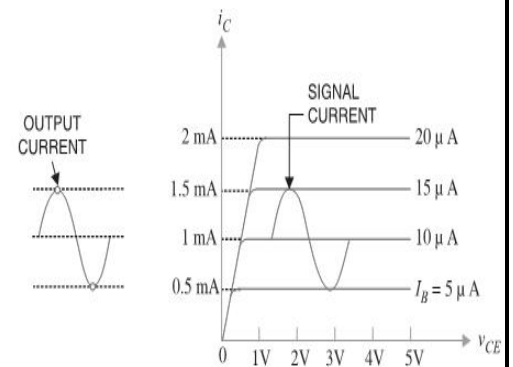
- A transistor circuit containing *more than one stage of amplification* is known as *multistage transistor amplifier*.
- In a multistage amplifier, a number of single amplifiers are connected in cascade arrangement i.e. output of first stage is connected to the input of the second stage through a suitable coupling device and so on.
- The purpose of **coupling device** (e.g. a capacitor, transformer etc.) is
  - (i) to transfer A.C. output of one stage to the input of the next stage and
  - (ii) to isolate the D.C. conditions of one stage from the next stage.
- The name of the amplifier is usually given after the type of coupling used. e.g.

Name of coupling	*Name of multistage amplifier*
RC coupling	R-C coupled amplifier
Transformer coupling	Transformer coupled amplifier
Direct coupling	Direct coupled amplifier

❖ IMPORTANT TERMS:-

➕ **Gain:** - The ratio of the output electrical quantity to the input one of the amplifier is called its gain.
- The gain of a multistage amplifier is equal to the product of gains of individual stages.
- For instance, if G_1, G_2 and G_3 are the individual voltage gains of a three-stage amplifier, then total voltage gain G is given by: $G = G_1 \times G_2 \times G_3$

➕ **Frequency response:** - The curve between voltage gain and signal frequency of an amplifier is known as frequency response.
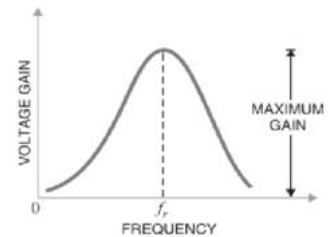- The gain of the amplifier increases as the frequency increases from zero till it becomes maximum at f_r, called resonant frequency.

➕ **Decibel gain:** - Although the gain of an amplifier can be expressed as a number, yet great practical importance to assign it a unit.
- The unit assigned is bel or decibel (db). The common logarithm (log to the base 10) of power gain is known as bel power gain i.e. Power gain $= \log_{10} \dfrac{P_{out}}{P_{in}} bel$ (1 bel=10 db.)

➕ Similarrly voltage gain and current gain may be defined as follows:-

$$\text{Voltage gain in } db = 10 \log_{10} \frac{V_{out}^2 / R}{V_{in}^2 / R} = 20 \log_{10} \frac{V_{out}}{V_{in}}$$

$$\text{Current gain in } db = 10 \log_{10} \frac{I_{out}^2 R}{I_{in}^2 R} = 20 \log_{10} \frac{I_{out}}{I_{in}}$$

➕ **Bandwidth:** - The range of frequency over which the voltage gain is equal to or greater than 70.7% of the maximum gain is known as **bandwidth**.
- From the fig. it is clear that for any frequency lying between f_1 and f_2, the gain is equal to or greater than 70.7% of the maximum gain.
- Therefore, $f_1 - f_2$ is the bandwidth. It may be seen that f_1 and f_2 are the limiting frequencies. The f_1 is called lower cut-off frequency and f_2 is known as upper cut-off frequency
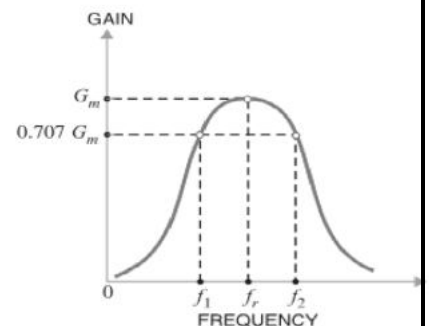
❖ R-C COUPLED TRANSISTOR AMPLIFIER:-

- This is the most popular type of coupling because it is cheap and *provides excellent audio fidelity over a wide range of frequency*. It is usually employed for **voltage amplification**.
- Fig shows two stages of an RC coupled amplifier. A coupling capacitor C_C is used to connect the output of first stage to the base (i.e. input) of the second stage and so on.
- As the coupling from one stage to next is achieved by a coupling capacitor followed by a connection to a shunt resistor, therefore, such amplifiers are called *Resistance - Capacitance coupled amplifiers*.

✐ The resistances R_1, R_2 and R_E form the *biasing* and *stabilization* network. The emitter bypass capacitor offers *low reactance path* to the signal. Without it, the voltage gain of each stage would be lost.

✐ The coupling capacitor C_C transmits A.C. signal but blocks D.C. This prevents D.C. interference between various stages and the shifting of operating point.
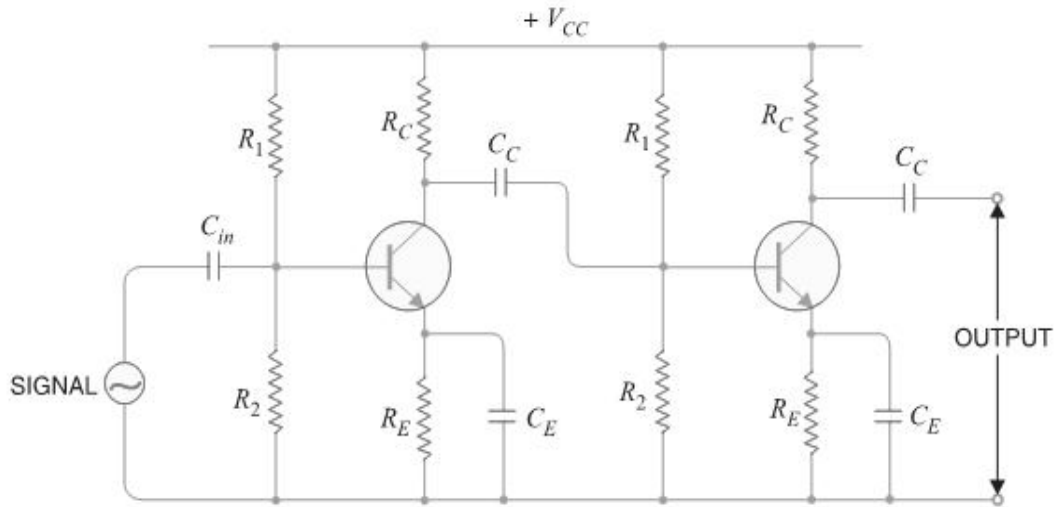
[Circuit Diagram of RC Coupled Transistor Amplifier]

✢ **Operation: -** When A.C. signal is applied to the base of the first transistor, it appears in the amplified form across its collector load R_C. The amplified signal developed across RC is given to base of next stage through coupling capacitor C_C. The second stage does further amplification of the signal. In this way, the cascaded (one after another) stages amplify the signal and the overall gain is considerably increased.

It may be mentioned here that total gain is less than the product of the gains of individual stages. It is because when a second stage is made to follow the first stage, the effective load resistance of first stage is reduced due to the shunting effect of the input resistance of second stage. This reduces the gain of the stage which is loaded by the next stage

✢ **FREQUENCY RESPONSE:**

✐ Fig shows the frequency response of a typical RC coupled amplifier. It is clear that voltage gain drops off at low (< 50 Hz) and high (> 20 kHz) frequencies whereas it is uniform over mid-frequency range (50 Hz to 20 kHz). This behaviour of the amplifier is briefly explained below:-

✐ **(i) At low frequencies** (< 50 Hz):- At this stage the reactance of coupling capacitor C_C is quite high and hence very small part of signal will pass from one stage to the next stage. Moreover, C_E cannot shunt the emitter resistance R_E effectively because of its large reactance at low frequencies. These two factors cause a falling of voltage gain at low frequencies.

✐ **(ii) At high frequencies** (> 20 kHz):-At this stage the reactance of C_C is very small and it behaves as a short circuit. These increases the loading effect of next stage and serves to reduce the voltage gain.

Moreover, at high frequency, capacitive reactance of base-emitter junction is low which increases the base current. This reduces the current amplification factor β. Due to these two reasons, the voltage gain drops off at high frequency. *[Frequency Response Curve of RC Coupled Amp]*
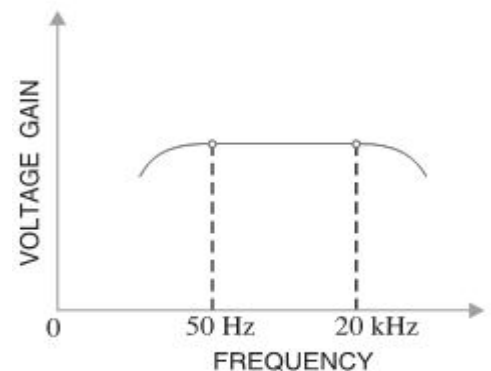
✐ **(iii) At mid-frequencies** (50 Hz to 20 kHz):- At this stage the voltage gain of the amplifier is constant. The effect of coupling capacitor in this frequency range is such so as to maintain a uniform voltage gain. Thus, as the frequency increases in this range, reactance of CC decreases which tends to increase the gain. However, at the same time, lower reactance means higher loading of first stage and hence lower gain. These two factors almost cancel each other, resulting in a uniform gain at mid-frequency.

✎ **Advantages:-**

(i) It has excellent frequency response. The gain is constant over the audio frequency range which is the region of most importance for speech, music etc.

(ii) It has lower cost since it employs resistors and capacitors which are cheap.

(iii) The circuit is very compact as the modern resistors and capacitors are small and extremely light.

✎ **Disadvantages:-**

(i) The RC coupled amplifiers have low voltage and power gain. It is because the low resistance presented by the input of each stage to the preceding stage decreases the effective load resistance (R_{AC}) and hence the gain.

(ii) They have the tendency to become noisy with age, particularly in moist climates.

(iii) Impedance matching is poor. It is because the output impedance of RC coupled amplifier is several hundred ohms whereas the input impedance of a speaker is only a few ohms. Hence, little power will be transferred to the speaker.

✎ **Applications:-**

✎ The RC coupled amplifiers have excellent audio fidelity over a wide range of frequency. Therefore, they are widely used as **voltage amplifiers** e.g. in the initial stages of public address system.

✎ If other type of coupling (e.g. transformer coupling) is employed in the initial stages, this results in frequency distortion which may be amplified in next stages.

✎ However, because of poor impedance matching, RC coupling is rarely used in the final stages.

✓ **Circuit diagram for Other Type of Coupling are given below:-**
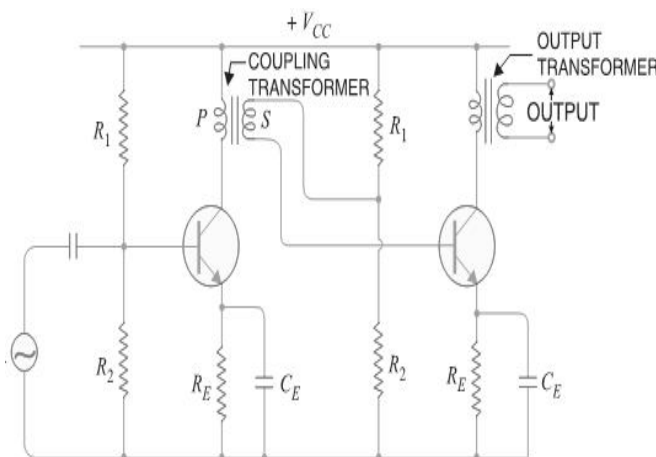
(Transformer Coupled Transistor Amplifier)   (Direct Coupled Transistor Amplifier)
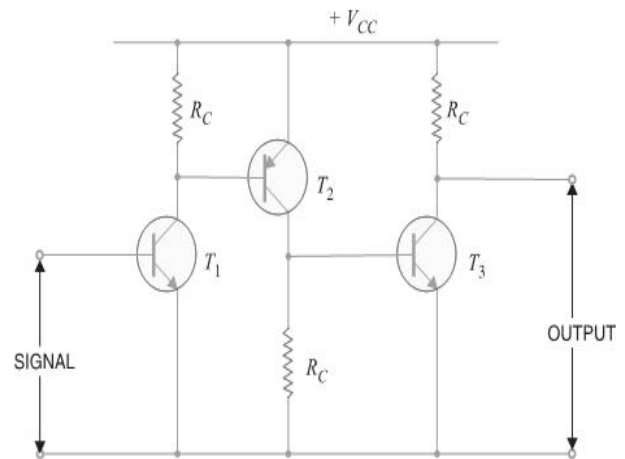
➢ **Comparison of Different Types of Coupling:-**

S. No	Particular	RC coupling	Transformer coupling	Direct coupling
1.	Frequency response	Excellent in the audio frequency range	Poor	Best
2.	Cost	Less	More	Least
3.	Space and weight	Less	More	Least
4.	Impedance matching	Not good	Excellent	Good
5.	Use	For voltage amplification	For power amplification	For amplifiying extremely low frequencies

❖ PHOTO TRANSISTOR: -

- ✎ It is light sensitive Transistor and is similar to an ordinary BJT except that it has no connection to the base terminal. Its operation is based on the photo diode that exits at CB junction.
- ✎ Instead of the base current, the input to the transistor is provided in the form of light as shown in symbol.
- ✎ Silicon NPNs are mostly used as photo Transistor. The device is usually is packed in a TO-type can with a lens on top although it is sometimes encapsulated in clear plastic.
- ✎ When there is no incident light on the CB junction, there is a small thermally generated collector-to-emitter leakage current I_{CEO} which, in this case is called **dark current** and is in the nA range.
- ✎ When light is incident on the CB junction, a base current I_λ is produced which is directly proportional to the light intensity. Hence, collector current $I_C = \beta I_\lambda$.
- ✎ Typical collector characteristic curve of a photo transistor are shown in fig. each individual curves corresponds to a certain value of light intensity expressed in mW/cm^2. As seen I_C increases with light intensity.
- ✎ The phototransistor has applications similar to those of a photo diode. Their main differences are in the current and response time. The photo transistor has the advantages of greater sensitivity and current capacity than photo diodes.
- ✎ However, photo diodes are faster of the two, switching in less than a nanosecond.
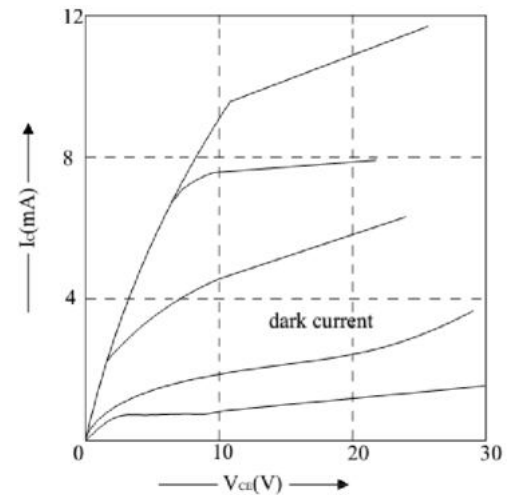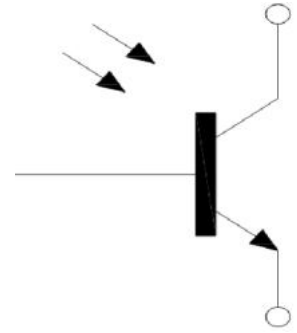
❖ PHOTO DARLINGTON: -

- ✎ As shown in fig. a Photo Darlington consists of a photo transistor in a Darlington arrangement with a common transistor.
- ✎ It has a much greater sensitivity to incident radiant energy than a photo transistor because of higher current gain.
- ✎ However, its switching time of 50μs is much longer than the photo transistor (2μs) or the photo diode (1ns). Its circuit symbol is shown in fig.
- ✎ Photo Darlington is used in a variety of application some of which are given below.
- ✎ A *light operated relay* in which the photo transistor Q_1 drives the bipolar transistor Q_2. When sufficient light falls on Q_1 it is driven into saturation so that I_C is increased multiple. This collector current while passing through the relay coil energizes the relay.
- ✎ A *dark operated relay* circuit i.e. one in which relay is deenergized when light falls on the photo transistor.
- ✎ Such relays are used in many applications such as
  (i) Automatic door activators
  (ii) Process Counters
 **(iii)** Various alarm systems for smoke or interference detection.
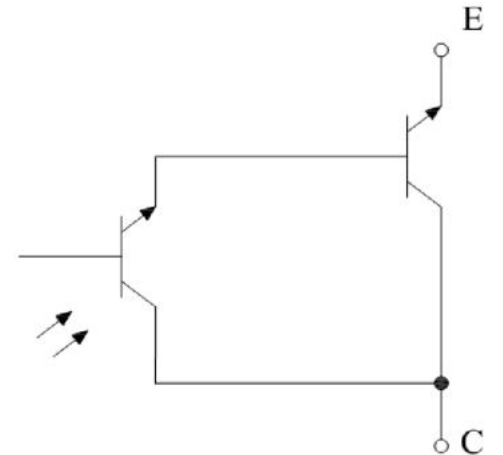
[CHAPTER-3]
-------------------------------- [AUDIO POWER AMPLIFIERS] --------------------------------

❖ **INTRODUCTION:-**

➢ A practical amplifier always consists of a number of stages that amplify a weak signal until sufficient power is available to operate a loudspeaker or other output device.

➢ The first few stages in this multistage amplifier have the function of only voltage amplification. However, last stage is designed to provide maximum power. This final stage is known as power stage.
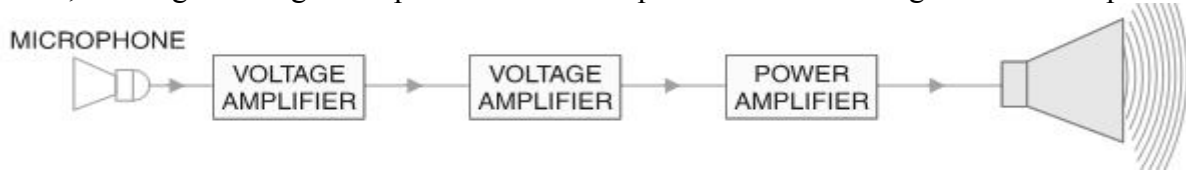
❖ **Transistor Audio Power Amplifier: -**

➢ A transistor amplifier which raises the power level of the signals having audio frequency range is known as transistor **Audio Power Amplifier**. Generally last stage of a multistage amplifier is the power stage.

➢ The power amplifier differs from all the previous stages in that here a concentrated effort is made to obtain maximum output power.

➢ A transistor that is suitable for power amplification is generally called a *power transistor*.

❖ **DIFFERENCE BETWEEN VOLTAGE AND POWER AMPLIFIERS**

➢ The difference between the two types is really one of degree; it is a question of how much voltage and how much power.

➢ A voltage amplifier is designed to achieve maximum voltage amplification. It is, however, not important to raise the power level.

➢ On the other hand, a power amplifier is designed to obtain maximum output power.

1) Voltage Amplifier. The voltage gain of an amplifier is given by : $A_v = \beta \times \dfrac{R_c}{R_{in}}$

➢ In order to achieve high voltage amplification, the following features are incorporated in such amplifiers:

♣ The transistor with high β(>100) is used in the circuit. i.e. Transistors are employed having thin base.

♣ The input resistance R_{in} of transistor is sought to be quite low as compared to the collector load R_C.

♣ A relatively high load R_C is used in the collector. To permit this condition, voltage amplifiers are always operated at low collector currents (≈ mA). If the collector current is small, we can use large R_C in the collector circuit

2) Power Amplifier. A power amplifier is required to deliver a large amount of power and as such it has to handle large current.

➢ In order to achieve high power amplification, the following features are incorporated in such amplifiers :

♣ The size of power transistor is made considerably larger in order to dissipate the heat produced in the transistor during operation.

♣ The base is made thicker to handle large currents. In other words, transistors with comparatively smaller β are used.

♣ Transformer coupling is used for impedance matching.

The comparison between voltage and power amplifiers is given below in the tabular form :

S. No.	Particular	Voltage amplifier	Power amplifier
1.	β	High (> 100)	low (5 to 20)
2.	R_C	High (4 – 10 kΩ)	low (5 to 20 Ω)
3.	*Coupling*	usually $R – C$ coupling	Invariably transformer coupling
4.	*Input voltage*	low (a few mV)	High (2 – 4 V)
5.	*Collector current*	low (≃ 1 mA)	High (> 100 mA)
6.	*Power output*	low	high
7.	*Output impedance*	High (≃ 12 kΩ)	low (200 Ω)

❖ **PERFORMANCE QUANTITIES OF POWER AMPLIFIERS**
➢ The prime objective for a power amplifier is to obtain maximum output power. Since a transistor, like any other electronic device has voltage, current and power dissipation limits, therefore, the criteria for a power amplifier are : **Collector Efficiency, Distortion & Power Dissipation Capability**
♣ **Collector efficiency.**
➢ The main criterion for a power amplifier is not the power gain rather it is the maximum a.c. power output. Now, an amplifier converts d.c. power from supply into a.c. power output.
➢ Therefore, the ability of a power amplifier to convert d.c. power from supply into a.c. output power is a measure of its effectiveness. This is known as *collector efficiency* and may be defined as under :
♣ The ratio of a.c. output power to the zero signal power (i.e. d.c. power) supplied by the battery of a power amplifier is known as **collector efficiency**.
♣ **Distortion.** The change of output wave shape from input wave shape of amplifier is called **Distortion**.
♣ **Power Dissipation Capability.** The ability of a power transistor to dissipate heat is known as power dissipation capability.

❖ **CLASSIFICATION OF POWER AMPLIFIERS**
➢ Transistor power amplifiers handle large signals. Many of them are driven by the input large signal that collector current is either cut-off or is in the saturation region during a large portion of the input cycle.
➢ Therefore, such amplifiers are generally classified according to their mode of operation i.e. the portion of the input cycle during which the collector current is expected to flow. On this basis, they are classified as
    (i) Class A power amplifier   **(ii)** Class B power amplifier   **(iii)** Class C power amplifier
♣ **CLASS A POWER AMPLIFIER.** If the collector current flows at all times during the full cycle of the signal, the power amplifier is known as *class A power amplifier*.
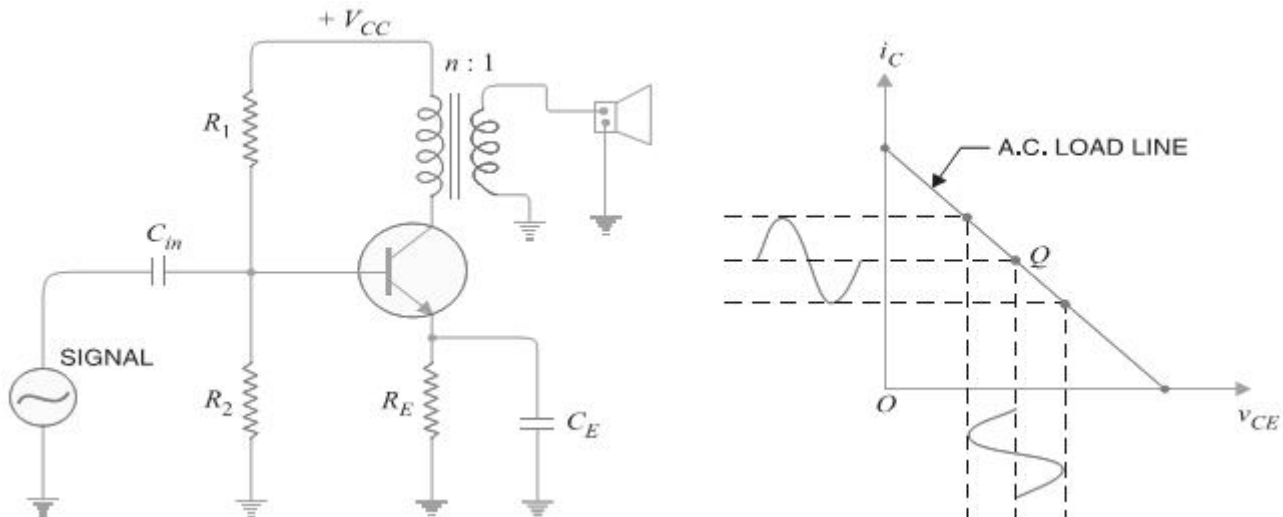
➢ The power amplifier must be biased in such a way that no part of the signal is cut off. Fig (i) shows circuit of class A power amplifier. Note that collector has a transformer as the load which is most common for all classes of power amplifiers.
➢ The use of transformer permits impedance matching, resulting in the transference of maximum power to the load e.g. loudspeaker. Fig (ii) shows the class A operation in terms of a.c. load line.
➢ The operating point Q is so selected that collector current flows at all times throughout the full cycle of the applied signal. As the output wave shape is exactly similar to the input wave shape, therefore, such amplifiers have least distortion.
➢ However, they have the disadvantage of low power output and low collector efficiency (about 35%).
♣ **CLASS B POWER AMPLIFIER**: - If the collector current flows only during the positive half-cycle of the input signal, it is called a *class B power amplifier*.
➢ In class B operation, the transistor bias is so adjusted that zero signal collector current is zero i.e. no biasing circuit is needed at all.
➢ During the positive half-cycle of the signal, the input circuit is forward biased and hence collector current flows. However, during the negative half-cycle of the signal, the input circuit is reverse biased and no collector current flows.

- Fig. shows the class B operation in terms of a.c. load line.
- The operating point Q shall be located at collector cut off voltage.
- It is easy to see that output from a class B amplifier is amplified half-wave rectification.
- In a class B amplifier, the negative half-cycle of the signal is cut off and hence a severe distortion occurs.
- However, class B amplifiers provide higher power output and collector efficiency $(50 - 60\%)$.
- Such amplifiers are mostly used for power amplification in push-pull arrangement.
- In such an arrangement, 2 transistors are used in class B operation. One transistor amplifies the positive half cycle of the signal while the other amplifies the negative half-cycle.
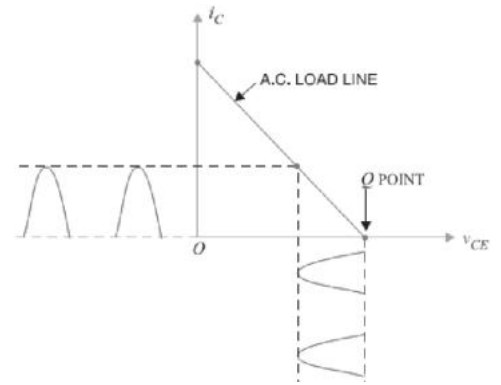
CLASS C POWER AMPLIFIER. If the collector current flows for less than half-cycle of the input signal, it is called *class C power amplifier*.

- In class C amplifier, the base is given some negative bias so that collector current does not flow just when the positive half-cycle of the signal starts.
- Such amplifiers are never used for power amplification. However, they are used as tuned amplifiers i.e. to amplify a narrow band of requencies near the resonant frequency.

EXPRESSION FOR COLLECTOR EFFICIENCY

- For comparing power amplifiers, collector efficiency is the main criterion. The greater the collector efficiency, the better is the power amplifier.
- Now, Collector Efficiency, $\boldsymbol{\eta} = \frac{a.c.\ power\ output}{d.c.\ power\ input} = \frac{P_O}{P_{dc}}$
- Where $P_{dc} = V_{CC}\ I_C$ & $P_O = V_{CE}\ I_C$ in which V_{CE} is the r.m.s. value of signal output voltage and I_c is the r.m.s. value of output signal current.
- In terms of peak-to-peak values, the a.c. power output can be expressed as:

$P_o = [(0.5 \times 0.707)\ v_{ce(p-p)}][(0.5 \times 0.707)\ i_{c(p-p)}] = \frac{v_{ce(p-p)} \times i_{c(p-p)}}{8}$ [As, $0.5 \times 0.707 \times 0.5 \times 0.707 = 0.125 = $**1/8**]

∴ **Collector $\eta = \frac{V_{ce(p-p)} \times i_{c(p-p)}}{8\ V_{cc}\ I_c}$**

MAXIMUM COLLECTOR EFFICIENCY OF SERIES-FED CLASS A AMPLIFIER : -

- Fig (i) shows a series fed class A amplifier. This circuit is seldom used for power amplification due to its poor collector efficiency.
- Nevertheless, it will help the reader to understand the class A operation. The d.c. load line of the circuit is shown in Fig. (ii).
- When an ac signal is applied to the amplifier, the output current and voltage will vary about the operating point Q.
- In order to achieve the maximum symmetrical swing of current and voltage (to achieve maximum output power), the Q point should be located at the centre of the dc load line.
- In that case, operating point is $I_C = V_{CC}/2R_C$ and $V_{CE} = V_{CC}/2$.
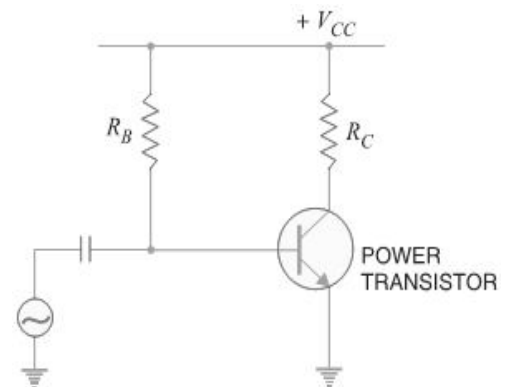
Maximum $v_{ce(p-p)} = V_{CC}$ Maximum $i_{c(p-p)} = V_{CC}/R_C$

Max. a.c. output power, $P_{o(max)} = \frac{v_{ce(p-p)} \times i_{c(p-p)}}{8} = \frac{V_{CC} \times V_{CC}/R_C}{8} = \frac{V_{CC}^2}{8R_C}$

D.C. power supplied, $P_{dc} = V_{CC}\ I_C = V_{CC}\left(\frac{V_{CC}}{2R_C}\right) = \frac{V_{CC}^2}{2R_C}$

∴ Maximum collector $\eta = \frac{P_{O\ (max)}}{P_{dc}} \times 100 = \frac{V_{CC}^2/8R_C}{V_{CC}^2/2R_C} \times 100 = $**25%**

- Thus the maximum collector efficiency of a class A series-fed amplifier is 25%.
- In actual practice, collector efficiency is far less than this value.
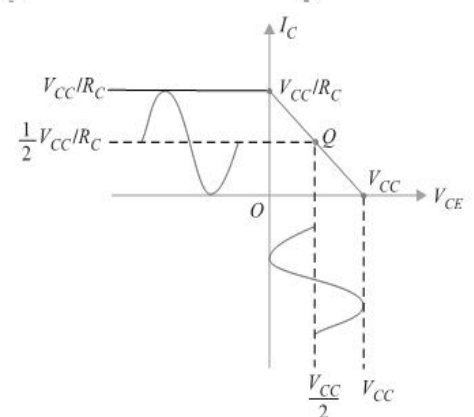
⊥ Maximum Collector Efficiency Of Transformer Coupled Class A Power Amplifier : -

➢ In class A power amplifier, the load can be either connected directly in the collector or it can be transformer coupled.

➢ But Transformer coupled method is often preferred for two main reasons. **First,** transformer coupling permits impedance matching. **Secondly** it keeps the d.c. power loss small because of the small resistance of the transformer primary winding.

➢ Fig(i) shows a transformer coupled class A power amplifier.

➢ In order to determine maximum collector efficiency, refer to the output characteristics shown in Fig (ii).

➢ Under zero signal conditions, the effective resistance in the collector circuit is that of primary winding of Transformer.

➢ The primary resistance has a very small value and is assumed zero. Therefore, d.c. load line is a vertical line rising from V_{CC} as shown in Fig. (ii).

➢ When signal is applied, the collector current will vary about the operating point Q.

➢ In order to get maximum a.c. power output (Hence maximum collector η), the peak value of collector current due to signal alone should be equal to the zero signal collector current I_C.

➢ In terms of a.c. load line, the operating point Q should be located at the centre of a.c. load line.

➢ During the peak of the positive half-cycle of the signal, the total collector current is $2 I_C$ and $v_{ce} = 0$. During the negative peak of the signal, the collector current is zero and $v_{ce} = 2V_{CC}$.

∴ Peak-to-peak collector-emitter voltage is
$$v_{ce(p-p)} = 2V_{CC}$$

Peak-to-peak collector current, $i_{c(p-p)} = 2 I_C = \frac{V_{ce(p-p)}}{R'_L} = \frac{2V_{cc}}{R'_L}$

Where R'_L is the reflected value of load R_L and appears in primary of the transformer.

➢ If n (= N_p/N_s) is the turn ratio of the transformer, then, $R'_L = n^2 R_L$.

➢ d.c. power input, $P_{dc} = V_{CC} I_C = I^2_C R'_L$ $\qquad\qquad$ (∵ $V_{CC} = I_C R'_L$)
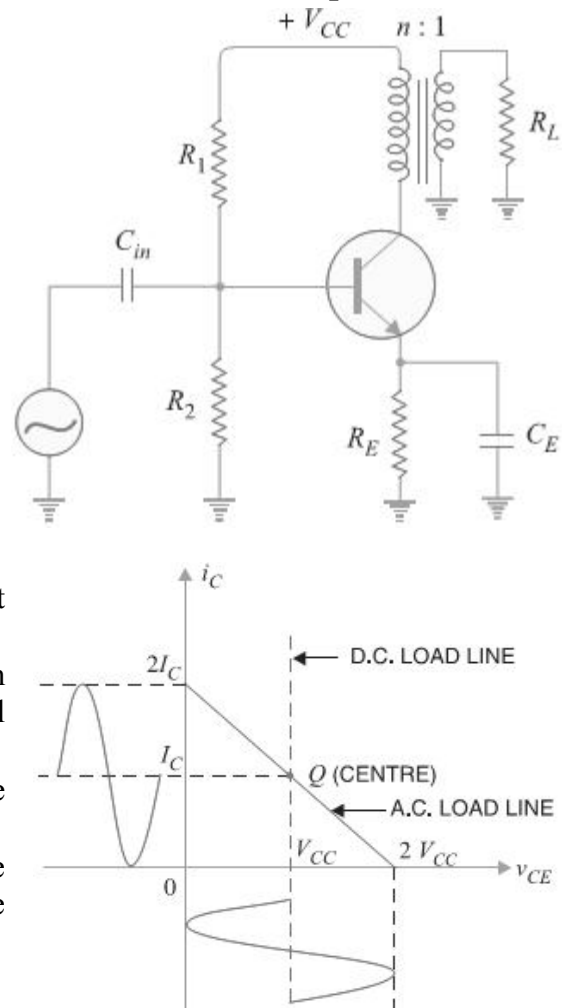
➢ Max. a.c. output power, $P_{o(max)} = \frac{V_{ce(p-p)} \times i_{c(p-p)}}{8} = \frac{2V_{CC} \times 2I_C}{8} = \frac{1}{2} V_{CC} I_C = \frac{1}{2} I^2_C R'_L$ … (i) (∵ $V_{CC} = I_C R'_L$)

∴ $\qquad$ Max. Collector η $= \frac{P_{O(max)}}{P_{dc}} \times 100 = \frac{\left(\frac{1}{2}\right)I^2_C R'_L}{I^2_C R'_L} \times 100 = $ **50%**

⊥ IMPORTANT POINTS ABOUT CLASS-A POWER AMPLIFIER : -

➢ **(i)** A Transformer coupled class A power amplifier has a maximum collector efficiency of 50% i.e., maximum of 50% d.c. supply power is converted into a.c. power output.

➢ In practice, the efficiency of such an amplifier is less than 50% (about 35%) due to power losses in the output transformer, power dissipation in the transistor etc.

➢ **(ii)** The power dissipated by a transistor is given by : $P_{dis} = P_{dc} - P_{ac}$
$\qquad\qquad$ Where $\quad$ Pdc= available d.c. power $\quad$ & $\quad$ P_{ac} = available a.c. power

➢ So, In class A operation, Transistor must dissipate less heat when signal is applied therefore runs cooler.

➢ **(iii)** When no signal is applied to a class A power amplifier, $P_{ac} = 0$. ∴ P_{dis}= Pdc

➢ Thus in class A operation, maximum power dissipation in the transistor occurs under zero signal conditions.

➢ Therefore, the power dissipation capability of a power transistor (for class A operation) must be at least equal to the zero signal rating.

➢ **(iv)** When a class A power amplifier used in final stage, it is called single ended class A power amplifier.

⊥ PUSH-PULL AMPLIFIER : -
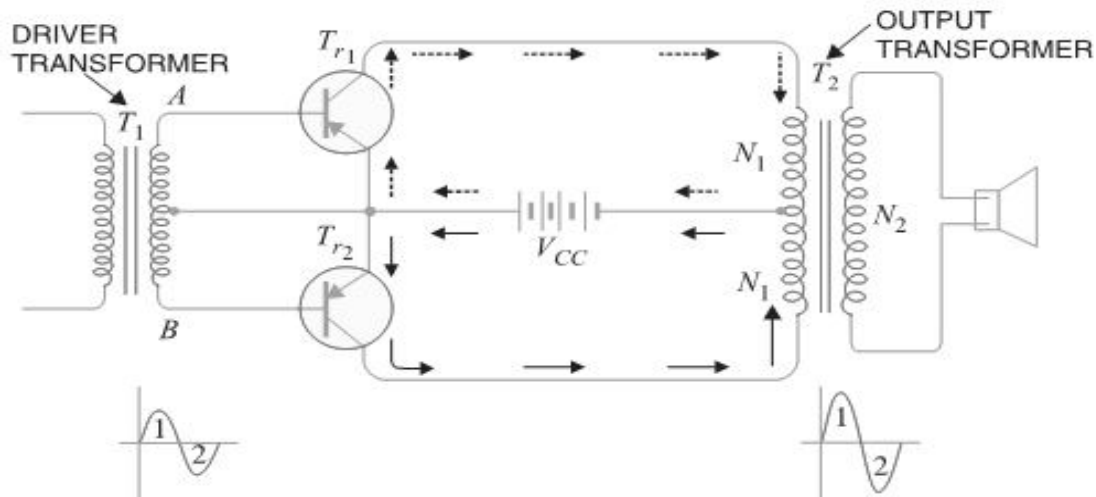
➤ The push-pull amplifier is a power amplifier and is frequently employed in the output stages of electronic circuits. It is used whenever high output power at high efficiency is required. Fig. shows the circuit of a push-pull amplifier.

➤ Two transistors T_{r1} and T_{r2} placed back to back are employed. Both transistors are operated in class B operation i.e. collector current is nearly zero in the absence of the signal.

➤ The centre tapped secondary of driver transformer T_1 supplies equal and opposite voltages to the base circuits of two transistors. The output transformer T_2 has the centre-tapped primary winding. The supply voltage V_{CC} is connected between the bases and this centre tap.

➤ The loudspeaker is connected across the secondary of this transformer.

⊥ CIRCUIT OPERATION.

➤ The input signal appears across the secondary AB of driver transformer. Suppose during the first half-cycle (marked 1) of the signal, end A becomes positive and end B negative.

➤ This will make the base-emitter junction of T_{r1} reverse biased and that of T_{r2} forward biased. The circuit will conduct current due to T_{r2} only and is shown by solid arrows.

➤ Therefore, this half-cycle of the signal is amplified by T_{r2} and appears in the lower half of the primary of output transformer. In the next half cycle of the signal, T_{r1} is forward biased whereas T_{r2} is reverse biased. Therefore, T_{r1} conducts and is shown by dotted arrows.

➤ Consequently, this half-cycle of the signal is amplified by T_{r1} and appears in the upper half of the output transformer primary. The centre-tapped primary of the output transformer combines two collector currents to form a sine wave output in the secondary.

➤ It may be noted here that push-pull arrangement also permits a maximum transfer of power to the Load through impedance matching. If R_L is the resistance appearing across secondary of output transformer, then resistance R'_L of primary shall become:

$$R'_L = \left(\frac{2N_1}{N_2}\right)^2 R_L$$

        Where N_1 = Number of turns between either end of primary winding and centre-tap

                         N_2 = Number of secondary turns

⊥ ADVANTAGES

1) The efficiency of the circuit is quite high (≈75%) due to class B operation.
2) A high a.c. output power is obtained.

⊥ DISADVANTAGES

1) Two transistors have to be used.
2) It requires two equal and opposite voltages at the input. Therefore, push-pull circuit requires the use of driver stage to furnish these signals.
3) If the parameters of the two transistors are not the same, there will be unequal amplification of the two halves of the signal.
4) The circuit gives more distortion.
5) Transformers used are bulky and expensive.

✚ MAXIMUM EFFICIENCY FOR CLASS B POWER AMPLIFIER

➢ We have already seen that a push-pull circuit uses two transistors working in class B operation. For class B operation, the Q-point is located at cut-off on both d.c. and a.c. load lines.

➢ For maximum signal operation, the two transistors in class B amplifier are alternately driven from cut-off to saturation. This is shown in Fig. (i). It is clear that a.c. output voltage has a peak value of V_{CE} and a.c. output current has a peak value of $I_{C(sat)}$.
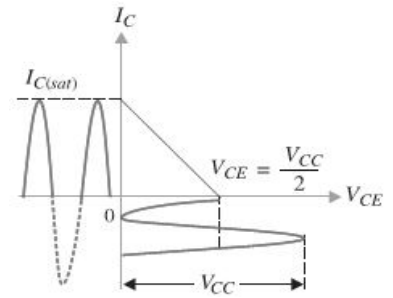
➢ The same information is also conveyed through the a.c. load line for the circuit [See Fig. (ii)].

∴   Peak a.c. output voltage = V_{CE}

Peak a.c. output current = $I_{C(sat)} = \frac{V_{CE}}{R_L} = \frac{V_{CC}}{2R_L}$ ($\because V_{CE} = \frac{V_{CC}}{2}$)

➢ Maximum average a.c. output power $P_{o\ (max)}$ is the Product of r.m.s. values of a.c. output voltage and a.c. output current

$$= \frac{V_{CE}}{\sqrt{2}} \times \frac{I_{C(sat)}}{\sqrt{2}} = \frac{V_{CE}I_{C(sat)}}{2} = \frac{V_{CC}}{2} \times \frac{I_{C(sat)}}{2} = \frac{V_{CC}I_{C(sat)}}{4} \quad (\because V_{CE} = \frac{V_{CC}}{2})$$
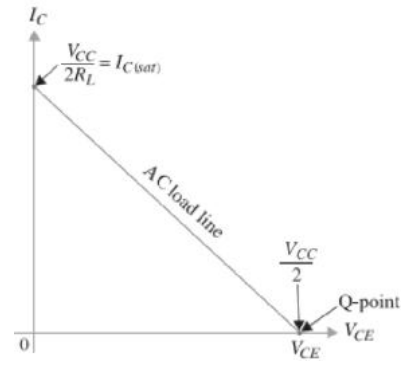
∴ $\mathbf{P_{o(max)} = 0.25\ V_{CC}I_{C(sat)}}$

➢ The input d.c. power from the supply V_{CC} is $\mathbf{P_{dc} = V_{CC}\ I_{dc}}$

Where I_{dc} is the average current drawn from the supply V_{CC}.

➢ Since the transistor is on for alternating half cycles, it effectively acts as a half-wave rectifier.

∴ $I_{dc} = \frac{I_{C(sat)}}{\pi}$ ➔ $P_{dc} = \frac{V_{CE}I_{C(sat)}}{\pi}$

∴   Max. Collector $\eta = \frac{P_{o\ (max)}}{P_{dc}} = \frac{0.25V_{CC}I_{C(sat)}}{(V_{CC}I_{C(sat)})/\pi} \times 100 = 0.25\pi \times 100 = \mathbf{78.5\ \%}$

➢ Thus the maximum collector efficiency of class B power amplifier is 78.5%. Recall that maximum collector efficiency for class A transformer coupled amplifier is 50%.

✚ COMPLEMENTARY-SYMMETRY AMPLIFIER

➢ By complementary symmetry is meant a principle of assembling push-pull class B amplifier without requiring centre-tapped transformers at the input and output stages.

➢ Fig. shows the transistor push-pull amplifier using complementary symmetry. It employs one npn and one pnp transistor and requires no centre-tapped transformers.

➢ The circuit action is as follows. During the positive-half of the input signal, transistor T_1 (the npn transistor) conducts current while T_2(the pnp transistor) is cutoff.

➢ During the negative half-cycle of the signal, T_2 conducts while T_1 is cut off. In this way, npn transistor amplifies the positive half-cycles of the signal while the pnp transistor amplifies the negative half-cycles of the signal.

➢ Note that we generally use an output transformer (not centre-tapped) for impedance matching.

✚ **Advantages: - (1)** This circuit does not require transformer. This saves on weight and cost.

               (2) Equal and opposite input signal voltages are not required.

✚ **Disadvantages:- (1)** It is difficult to get a pair of transistors (npn & pnp) having similar characteristics.

               (2) We require both positive and negative supply voltages.

✚ HEAT SINK: -

➢ As power transistors handle large currents, they always heat up during operation. Since transistor is a temperature dependent device, the heat must be dissipated to the surroundings to keep the temperature within allowed limits.

➢ Usually transistor is fixed on Aluminum metal sheet so that additional heat is transferred to the Al sheet.

➢ The metal sheet that serves to dissipate the additional heat from power transistor is known as **Heat Sink.**
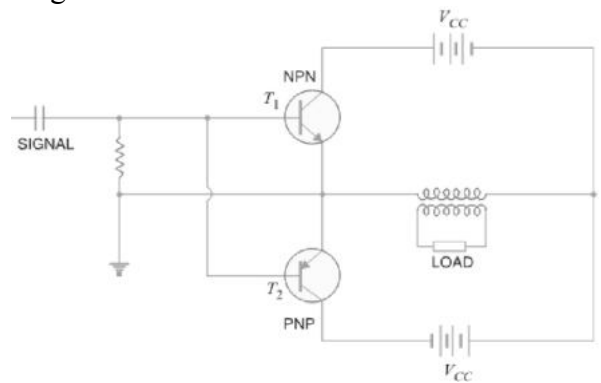
[CHAPTER-4]

----------------------- [FIELD EFFECT TRANSISTOR (FET)] -----------------------

❖ **INTRODUCTION: -**

➢ In the previous chapters, we have discussed the circuit applications of an ordinary transistor. In this type of transistor, both holes and electrons play part in the conduction process. For this reason, it is sometimes called a **Bipolar Transistor.**

➢ The ordinary or bipolar transistor has two principal disadvantages. **First**, it has low input impedance because of forward biased emitter junction. **Secondly**, it has considerable noise level.

➢ Although low input impedance problem may be improved by careful design and use of more than one transistor, yet it is difficult to achieve input impedance more than a few mega ohms.

➢ The field effect transistor (FET) has, by virtue of its construction and biasing, large input impedance which may be more than 100 mega ohms.

➢ The FET is generally much less noisy than the ordinary or bipolar transistor. The rapidly expanding FET market has led many semiconductor marketing managers to believe that this device will soon become the most important electronic device, primarily because of its integrated-circuit applications.

❖ **CLASSIFICATION OF FIELD EFFECT TRANSISTORS: -**
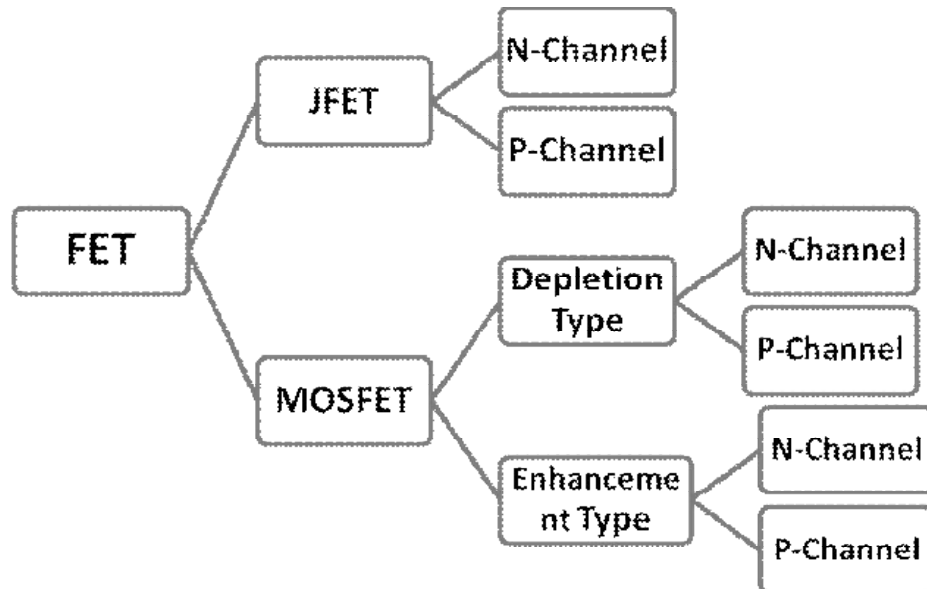
❖   Other types of C-MOS also There Such as: -**CMOS, VMOS, LDMOS** etc.

❖ **DIFFERENTIATION BETWEEN BJT & FET : -**

FET	BJT
✖ It means **Field Effect Transistor**	✖ Means **Bipolar Junction Transistor**
✖ Its three terminals are **Source, Gate & Drain**	✖ Its terminals are **Emitter, Base & Collector.**
✖ It is **Unipolar** devices i.e. Current in the device is carried either by electrons or holes.	✖ It is **Bipolar** devices i.e. Current in the device is carried by both electrons and holes.
✖ It is **Voltage controlled device.** i.e. Voltage at the gate or drain terminal controls the amount of current flowing through the devices.	✖ It is **Current controlled device.** i.e. Base Current controls the amount of collector current flowing through the devices.
✖ It has very High Input Resistance and Low Output Resistance.	✖ It has very Low Input Resistance and High Output Resistance.
✖ Low noisy operation	✖ High noisy operation
✖ It is Longer Life & High Efficiency.	✖ It is Shorter Life & Low Efficiency.
✖ It is much simpler to fabricate as IC and occupies less space on IC.	✖ It is comparatively difficult to fabricate as IC and occupies more space on IC then FET.
✖ It has Small gain bandwidth product.	✖ It has Large gain bandwidth product.
✖ It has higher switching speed.	✖ It has higher switching speed.

❖ JUNCTION FIELD EFFECT TRANSISTOR (JFET) : -

➢ A junction field effect transistor is a three terminal semiconductor device in which current conduction is by one type of carrier i.e., electrons or holes.

➢ In a JFET, the current conduction is either by electrons or holes and is controlled by means of an electric field between the gate electrode and the conducting channel of the device.

➢ The JFET has high input impedance and low noise level.

❖ CONSTRUCTIONAL DETAILS.

➢ A JFET consists of a p-type or n-type silicon bar containing two pn junctions at the sides as shown in Fig.

➢ The bar forms the conducting channel for the charge carriers. If the bar is of n-type, it is called n-channel JFET as shown in Fig (i) and if the bar is of p-type, it is called a p-channel JFET as shown in Fig (ii).

➢ The two pn junctions forming diodes are connected internally & a common terminal called **gate** is taken out.

➢ Other terminals are **source** and **drain** taken out from the bar as shown. Thus a JFET has essentially three terminals viz., Gate (G), Source (S) & Drain (D).
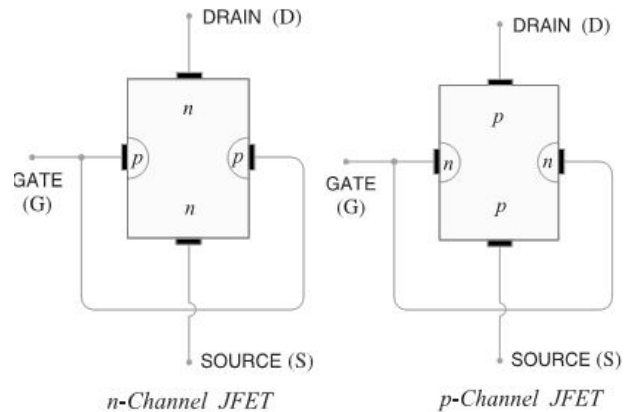
❖ JFET POLARITIES: -

➢ Fig (i) shows n-channel JFET polarities whereas Fig (ii) shows the p-channel JFET polarities.

➢ Note that in each case, voltage between gate and source is such that the gate is reversing biased.

➢ This is the normal way of JFET connection.

➢ The drain & source terminals are interchangeable i.e., either end can be used as source and the other end as drain.
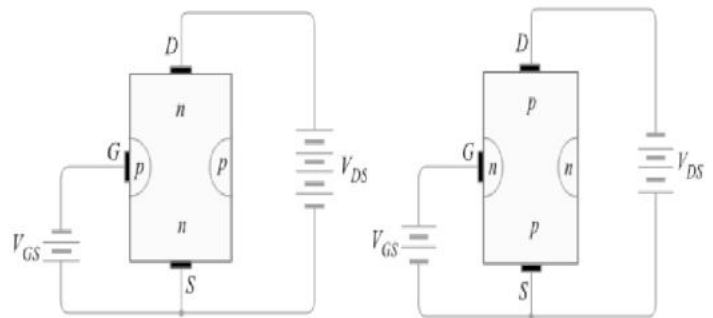
➢ The following points may be noted:

♣ The input circuit (i.e. gate to source) of a JFET is reverse biased. This means that the device has high input impedance.

♣ The drain is so biased w.r.t. source that drain current I_D flows from the source to drain.

♣ In all JFETs, source current I_S is equal to the drain current i.e. $I_S = I_D$.

❖ WORKING PRINCIPLE OF JFET:-

➕ **Principle: –** Fig. shows the circuit of n-channel JFET with normal polarities. Note that the gate is reverse biased.

➢ The two pn junctions at the sides form two depletion layers. The current conduction by charge carriers (i.e. free electrons in this case) is through the channel between the two depletion layers and out of the drain.
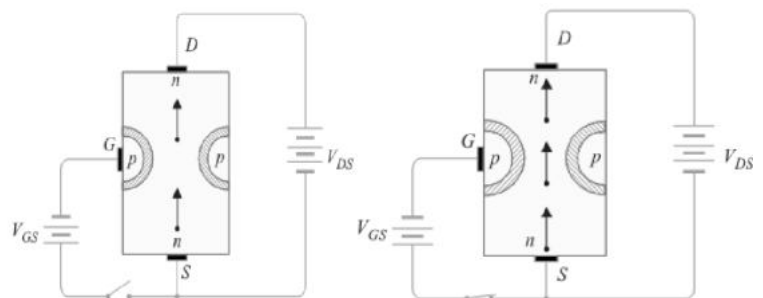
➢ The width and hence resistance of this channel can be controlled by changing the input voltage V_{GS}.

➢ The greater the reverse voltage V_{GS}, the wider will be the depletion layers and narrower will be the conducting channel. The narrower channel means greater resistance and hence source to drain current decreases. Reverse will happen should V_{GS} decrease.

➢ Thus JFET operates on the principle that width and hence resistance of the conducting channel can be varied by changing the reverse voltage V_{GS}.

➢ In other words, the magnitude of drain current (I_D) can be changed by altering V_{GS}.

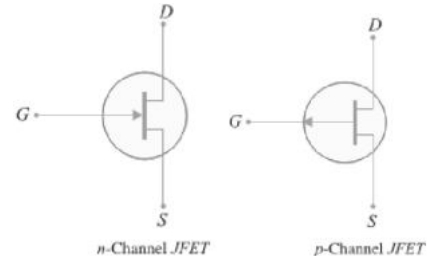➕ **Working: –** The working of JFET is as under :

➢ **(i)** When voltage V_{DS} is applied between drain & source terminals and voltage on the gate is zero [See the above Fig (i)], the two pn junctions at the sides of the bar establish depletion layers.

➢ The electrons will flow from source to drain through a channel between the depletion layers.

➤ The size of these layers determines width of the channel & hence the current conduction through the bar.
➤ **(ii)** When a reverse voltage V_{GS} is applied between the gate and source [See Fig (ii)], the width of the depletion layers is increased.
➤ This reduces the width of conducting channel, thereby increasing the resistance of n-type bar. Consequently, the current from source to drain is decreased.
➤ On the other hand, if the reverse voltage on the gate is decreased, the width of the depletion layers also decreases. This increases the width of the conducting channel and hence source to drain current.
➤ It is clear from the above discussion that current from source to drain can be controlled by the application of potential (i.e. electric field) on the gate.
➤ For this reason, the device is called field effect transistor. It may be noted that a p-channel JFET operates in the same manner as an n-channel JFET except that channel current carriers will be the holes instead of electrons and the polarities of V_{GS} and V_{DS} are reversed.

❖ **JFET AS AN AMPLIFIER :-**

➤ Fig shows JFET amplifier circuit. The weak signal is applied between gate and source and amplified output is obtained in the drain-source circuit. For the proper operation of JFET, the gate must be negative w.r.t. source i.e., input circuit should always be reverse biased.
➤ This is achieved either by inserting a battery V_{GG} in the gate circuit or by a circuit known as biasing circuit.

[Schematic Symbol of JFET]

➤ In the present case, we are providing biasing by the battery V_{GG}. A small change in the reverse bias on the gate produces a large change in drain current.
➤ This fact makes JFET capable of raising the strength of a weak signal. During the positive half of signal, the reverse bias on the gate decreases. This increases the channel width and hence the drain current.
➤ During the negative half-cycle of the signal, the reverse voltage on the gate increases. Consequently, the drain current decreases.
➤ The result is that a small change in voltage at the gate produces a large change in drain current.
➤ These large variations in drain current produce large output across the load R_L. In this way, JFET acts as an amplifier
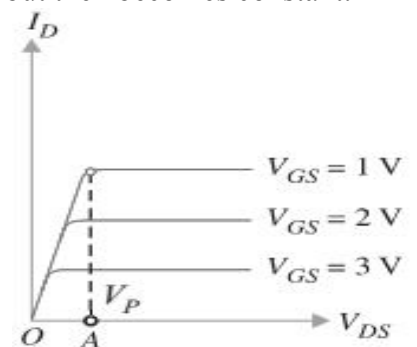
❖ **OUTPUT CHARACTERISTICS OF JFET**

➤ The curve between drain current (I_D) and drain-source voltage (V_{DS}) of a JFET at constant gate source voltage (V_{GS}) is known as output characteristics of JFET.
➤ Fig shows circuit for determining output characteristics of JFET.
➤ Keeping V_{GS} fixed at some value, say 1V, the drain source voltage is changed in steps.
➤ Corresponding to each value of V_{DS}, the drain current I_D is noted.
➤ A plot of these values gives output characteristic of JFET at $V_{GS}= 1V$.
➤ Repeating similar procedure, output characteristics at other gate-source voltages can be drawn. Fig. shows a family of output characteristics.
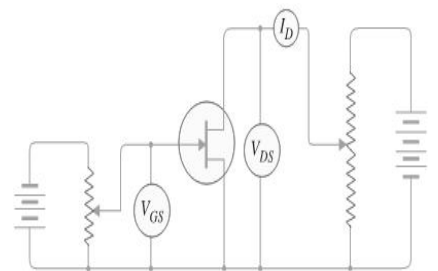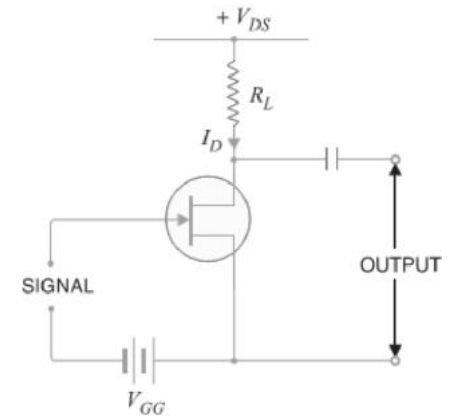
🔸 **The following points may be noted from the characteristics:**

➤ **(i)** At first, the drain current I_D rises rapidly with drain-source voltage V_{DS} but then becomes constant.
➤ The drain-source voltage above which drain current becomes constant is known as pinch off voltage. Thus in Fig. OA is the pinch off voltage V_P.
➤ **(ii)** After pinch off voltage, the channel width becomes so narrow that depletion layers almost touch each other.
➤ The drain current passes through the small passage between these layers.
➤ Thus increase in drain current is very small with V_{DS} above pinch off voltage.
➤ Consequently, drain current remains constant. The characteristics resemble that of a pentode valve.

🞂 **SALIENT FEATURES OF JFET : -**
➢ The following are some salient features of JFET:
  ♣ **(i)** A JFET is a three-terminal voltage-controlled semiconductor device i.e. input voltage controls the output characteristics of JFET.
  ♣ **(ii)** The JFET is always operated with gate-source pn junction reverse biased.
  ♣ **(iii)** In a JFET, the gate current is zero i.e. $I_G = 0A$. **(iv)** Since there is no gate current, $I_D = I_S$
  ♣ **(v)** The JFET must be operated between V_{GS} and V_{GS} (off). For this range of gate-to-source voltages, I_D will vary from a maximum of I_{DSS} to a minimum of almost zero.
  ♣ **(vi)** As two gates are the same potential, both depletion layers widen or narrow by an equal amount.
  ♣ **(vii)** The JFET is not subjected to thermal runaway when the temperature of the device increases.
  ♣ **(viii)** The drain current I_D is controlled by changing the channel width.
  ♣ **(ix)** Since JFET has no gate current, there is no β rating of the device. We can find drain current I_D

🞂 **IMPORTANT TERMS : -**
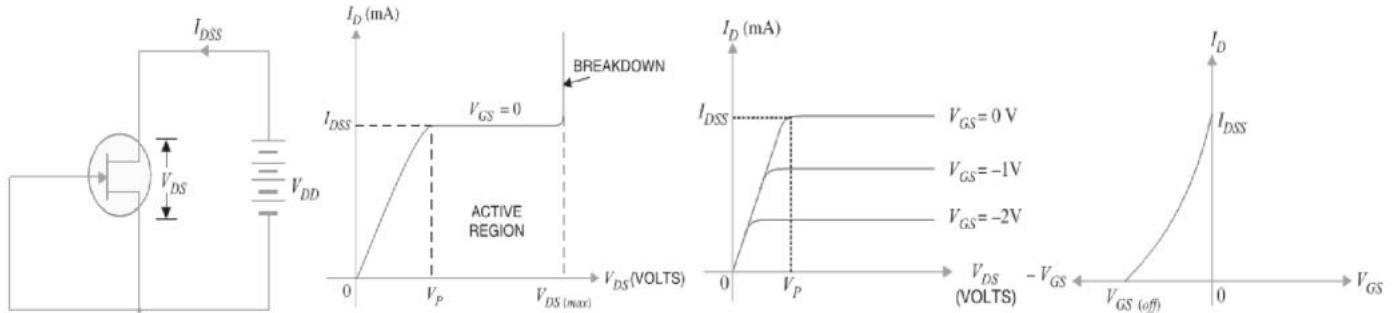
  1. Shorted-Gate Drain Current (I_{DSS}): -
➢ It is the drain current with source short-circuited to gate (i.e. $V_{GS} = 0$) and drain voltage (V_{DS}) equal to pinch off voltage. It is sometimes called zero-bias current.
  2. Pinch Off Voltage (V_P) : -
➢ It is the minimum drain-source voltage at which the drain current essentially becomes constant.
  3. Gate-Source Cut Off Voltage V_{GS} (off): -
➢ It is the gate-source voltage where the channel is completely cut off and the drain current becomes zero.

❖ **PARAMETERS OF JFET: -**
➢ Like vacuum tubes, a JFET has certain parameters which determine its performance in a circuit. The main parameters of JFET are: - **(i)** A.C. drain resistance **(ii)** Transconductance **(iii)** Amplification factor.
  ♣ **(i)** <u>A.C. Drain Resistance</u> (**r$_d$**). Corresponding to the a.c. plate resistance, we have a.c. drain resistance in a JFET. It may be defined as follows :
➢ It is the ratio of change in drain-source voltage (ΔV_{DS}) to the change in drain current(ΔI_D) at constant gate-source voltage i.e.

$$\boxed{\text{A.C. Drain Resistance, } r_d = \frac{\Delta V_{DS}}{\Delta I_D} \text{ at constant } V_{GS}}$$

➢ For instance, if a change in drain voltage of 2 V produces a change in drain current of 0.02 mA, then, a.c. drain resistance, $r_d = \frac{2V}{0.02\ mA} = 100\ k\Omega$
➢ Referring to the output characteristics of a JFET in Fig., it is clear that above the pinch off voltage, the change in I_D is small for a change in V_{DS} because the curve is almost flat.
➢ Therefore, drain resistance of a JFET has a large value, ranging from 10 kΩ to 1 MΩ.
  ♣ **(ii)** <u>Transconductance</u> (**g$_{fs}$**) : -The control that the gate voltage has over the drain current is measured by transconductance g_{fs} & is similar to the transconductance g_m of the tube. It may be defined as follows :
➢ It is the ratio of change in drain current (ΔI_D) to the change in gate-source voltage(ΔV_{GS}) at constant drain-source voltage i.e.

$$\boxed{\text{Transconductance, } g_{fs} = \frac{\Delta I_D}{\Delta V_{GS}} \text{ at constant } V_{DS}}$$

➢ The transconductance of a JFET is usually expressed either in mA/volt or micro mho. As an example, if a change in gate voltage of 0.1 V causes a change in drain current of 0.3 mA, then, Transconductance,
  ➔ $g_{fs} = \frac{0.3\ mA}{0.1\ V} = 3mA/V = 3 \times 10^{-3}$ A/V or mho or S(Siemens)$= 3 \times 10^{-3} \times 10^6\ \mu$ mho = 3000 μ mho (or μS)

♣ **(iii) <u>Amplification Factor</u> (μ)**. It is the ratio of change in drain-source voltage (ΔV_{DS}) to the change in gate-source voltage(ΔV_{GS}) at constant drain current i.e.

$$\boxed{\textbf{Amplification Factor, } \mu = \frac{\Delta V_{DS}}{\Delta V_{GS}} \textbf{ at constant } I_D}$$

➢ Amplification factor of a JFET indicates how much more control the gate voltage has over drain current than has the drain voltage.

➢ For instance, if the amplification factor of a JFET is 50, it means that gate voltage is 50 times as effective as the drain voltage in controlling the drain current.

❖ **RELATION AMONG JFET PARAMETERS: -**

➢ The relationship among JFET parameters can be established as under :

$$\textbf{We know} \quad \mu = \frac{\Delta V_{DS}}{\Delta V_{GS}}$$

➢ Multiplying the numerator and denominator on R.H.S. by ΔI_D, we get,

$$\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}} \times \frac{\Delta I_D}{\Delta I_D} = \frac{\Delta V_{DS}}{\Delta I_D} \times \frac{\Delta I_D}{\Delta V_{GS}} \qquad \rightarrow \qquad \boxed{\mathbf{\mu = r_d \times g_{fs}}}$$

$$\boxed{\rightarrow \textbf{ Amplification Factor = A.C. Drain Resistance × Transconductance}}$$

❖ **JFET BIASING: -**

➢ For the proper operation of n-channel JFET, gate must be negative w.r.t. source. This can be achieved either by inserting a battery in the gate circuit or by a circuit known as biasing circuit.

➢ The latter method is preferred because batteries are costly and require frequent replacement.
1. Bias battery: - In this method, JFET is biased by a bias battery V_{GG}. This battery ensures that gate is always negative w.r.t. source during all parts of the signal.
2. Biasing circuit: -The biasing circuit uses supply voltage V_{DD} to provide the necessary bias. Two most commonly used methods are **(i) Self-Bias (ii) Potential Divider Method**.

❖ **SELF-BIAS FOR JFET : -**

➢ Fig shows the self-bias method for n-channel JFET. The resistor RS is the bias resistor.

➢ The d.c. component of drain current flowing through R_S produces the desired bias voltage.

$$\text{Voltage across } R_S, \ V_S = I_D R_S$$

➢ Since gate current is negligibly small, the gate terminal is at d.c. ground i.e., $V_G = 0$.

$$\therefore \quad V_{GS} = V_G - V_S = 0 - I_D R_S \quad \text{or} \quad V_{GS} = - I_D R_S$$

➢ Thus bias voltage V_{GS} keeps gate negative w.r.t. source.

♦ **Operating point: -**

➢ The operating point (i.e., zero signals I_D & V_{DS}) can be easily determined. Since the parameters of the JFET are usually known, zero signal I_D can be calculated from the following relation :

$$\mathbf{I_D = I_{DSS} \left(1 - \frac{\Delta V_{GS}}{\Delta V_{GS\,(off)}}\right)^2}$$

Also $\qquad\qquad V_{DS} = V_{DD} - I_D (R_D + R_S)$

➢ Thus d.c. conditions of JFET amplifier are fully specified i.e. operating point for the circuit is (V_{DS}, I_D).

Also, $\qquad\qquad \mathbf{R_S = \frac{|V_{GS}|}{|I_D|}}$

➢ Note that gate resistor R_G does not affect bias because voltage across it is zero.

♦ **Midpoint Bias: -** It is often desirable to bias a JFET near the midpoint of its transfer characteristic curve where $I_D = I_{DSS}/2$. When signal is applied, the midpoint bias allows a maximum amount of drain current swing between I_{DSS} and 0.

➢ It can be proved that when $V_{GS} = V_{GS\,(off)} / 3.4$, midpoint bias conditions are obtained for I_D.

$$I_D = I_{DSS} \left(1 - \frac{\Delta V_{GS}}{\Delta V_{GS\,(off)}}\right)^2 = I_{DSS} \left(1 - \frac{\Delta V_{GS\,(off)}/3.4}{\Delta V_{GS(off)}}\right)^2 = 0.5 \ I_{DSS}$$

➢ To set drain voltage at midpoint ($V_D = V_{DD}/2$), select a value of R_D to produce the desired voltage drop.
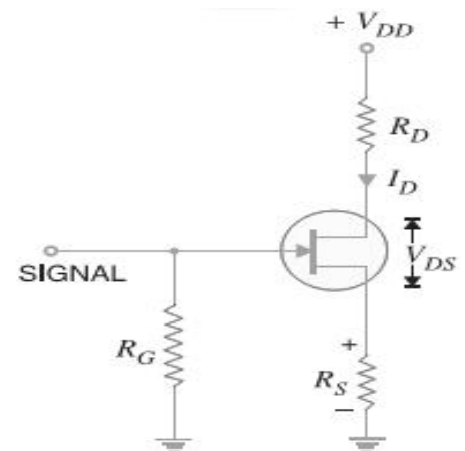
❖ **JFET with Voltage-Divider Bias :-**

➢ Fig shows potential divider method of biasing a JFET. This circuit is identical to that used for a transistor.

➢ The resistors R_1 and R_2 form a voltage divider across drain supply V_{DD}. The voltage V_2 (= V_G) across R_2 provides the necessary bias.

$$V_2 = V_G = \frac{V_{DD}}{R_1 + R_2} \times R_2$$

Now $\qquad V_2 = V_{GS} + I_D R_S \qquad$ Or $\qquad$ **$V_{GS} = V_2 - I_D R_S$**

➢ The circuit is so designed that $I_D R_S$ is larger than V_2 so that V_{GS} is negative. This provides correct bias voltage. We can find the operating point as under:

$$I_D = \frac{V_2 - V_{GS}}{R_s} \quad \text{and} \quad V_{DS} = V_{DD} - I_D (R_D + R_S)$$

➢ Although the circuit of voltage-divider bias is a bit complex, yet the advantage of this method of biasing is that it provides good stability of the operating point.

➢ The input impedance Z_i of this circuit is given by ; $\qquad Z_i = R_1 \parallel R_2$

❖ **JFET Connections: -**

➢ There are three leads in a JFET viz., source, gate and drain terminals. However, when JFET is to be connected in a circuit, we require four terminals; two for the input and two for the output.

➢ This difficulty is overcome by making one terminal of the JFET common to both input and output terminals. Accordingly, a JFET can be connected in a circuit in the following three ways:

   ♣ Common Source connection
   ♣ Common Gate connection
   ♣ Common Drain connection

➢ The common source connection is the most widely used arrangement. It is because this connection provides high input impedance, good voltage gain and moderate output impedance.

➢ However, the circuit produces a phase reversal i.e., output signal is 180° out of phase with the input signal. Fig. shows a common source n-channel JFET amplifier.

➢ Note that source terminal is common to both input and output.

✚ **JFET Applications : -**

➢ The high input impedance and low output impedance and low noise level make JFET far superior to the bipolar transistor. Some of the circuit applications of JFET are :

   ♣ As a Buffer amplifier
   ♣ As Phase-shift oscillators
   ♣ As RF amplifier

❖ **Metal Oxide Semiconductor FET (MOSFET) :-**

➢ The main drawback of JFET is that its gate must be reverse biased for proper operation of the device i.e.it can only have negative gate operation for n-channel and positive gate operation for p-channel.

➢ This means that we can only decrease the width of the channel (i.e. decrease the conductivity of the channel) from its zero-bias size.

➢ This type of operation is referred to as depletion-mode operation. Therefore, a JFET can only be operated in the depletion-mode.

➢ However, there is a field effect transistor (FET) that can be operated to enhance (or increase) the width of the channel (with consequent increase in conductivity of the channel) i.e. it can have enhancement-mode operation. Such a FET is called **MOSFET.**

➢ A field effect transistor (FET) that can be operated in the enhancement-mode is called a **MOSFET**.

➢ A MOSFET is an important semiconductor device & can be used in any of the circuits covered for JFET.
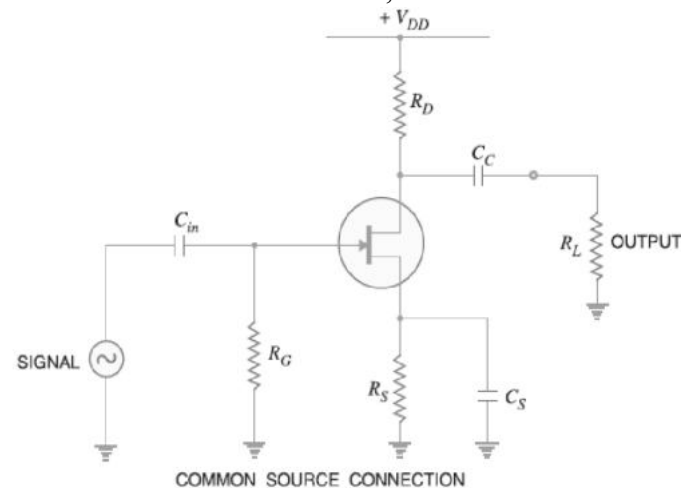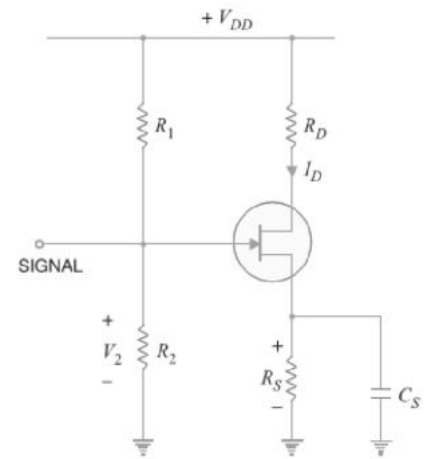
➢ However, a MOSFET has several advantages over JFET including high input impedance and low cost.

❖ **TYPES OF MOSFETS :-**

➢ There are two basic types of MOSFETs such as: -

1. Depletion-type MOSFET or D-MOSFET. The D-MOSFET can be operated in both the depletion mode and the enhancement-mode.

  ➢ For this reason, a D-MOSFET is sometimes called **Depletion/Enhancement MOSFET**.

2. Enhancement-type MOSFET or E-MOSFET. The E-MOSFET can be operated only in enhancement mode. The manner in which a MOSFET is constructed determines whether it is D-MOSFET or E-MOSFET.

❖ **D-MOSFET.** Fig shows the constructional details of n-channel D-MOSFET.

➢ It is similar to n-channel JFET except with the following modifications/remarks :

➢ **(i)** The n-channel D-MOSFET is a piece of n-type material with a p-type region (called substrate) on the right and an insulated gate on the left as shown in Fig.

➢ The free electrons (Q it is n-channel) flowing from source to drain must pass through the narrow channel between the gate and the p-type region (i.e. substrate).

➢ **(ii)** Note carefully the gate construction of D-MOSFET. A thin layer of metal oxide (usually silicon dioxide, SiO_2) is deposited over a small portion of the channel.

➢ A metallic gate is deposited over the oxide layer. As SiO_2 is an insulator, thus gate is insulated from the channel. Note that the arrangement forms a capacitor. One plate of this capacitor is the gate and other plate is the channel with SiO_2 as dielectric. Recall that we have a gate diode in a JFET.

n-Channel D-MOSFET

➢ **(iii)** It is a usual practice to connect the substrate to the source (S) internally so that a MOSFET has three terminals viz Source (S), Gate (G) and Drain (D).

➢ **(iv)** Since the gate is insulated from the channel, we can apply either negative or positive voltage to the gate. Therefore, D-MOSFET can be operated in both depletion-mode and enhancement-mode. However, JFET can be operated only in depletion-mode.

❖ **E-MOSFET**. Fig shows the constructional details of n-channel E-MOSFET. Its gate construction is similar to that of D-MOSFET.

➢ The E-MOSFET has no channel between source and drain unlike the D-MOSFET. Note that the substrate extends completely to the SiO_2 layer so that no channel exists.

➢ The E-MOSFET requires a proper gate voltage to form a channel (called induced channel). It is reminded that E-MOSFET can be operated only in enhancement mode.

➢ In short, the construction of E-MOSFET is quite similar to that of the D-MOSFET except for the absence of a channel between the drain and source terminals.

n-Channel E-MOSFET

❖ **Why the name MOSFET ?**

➢ The reader may wonder why is the device called MOSFET?

➢ The answer is simple. The SiO_2 layer is an insulator. The gate terminal is made of a metal conductor.

➢ Thus, going from gate to substrate, we have a metal oxide semiconductor and hence the name MOSFET.
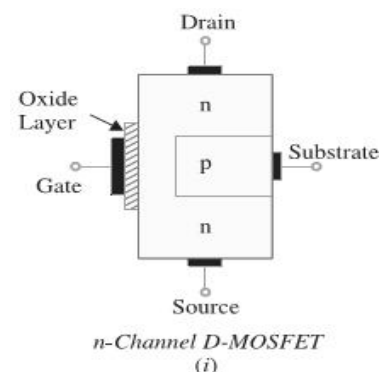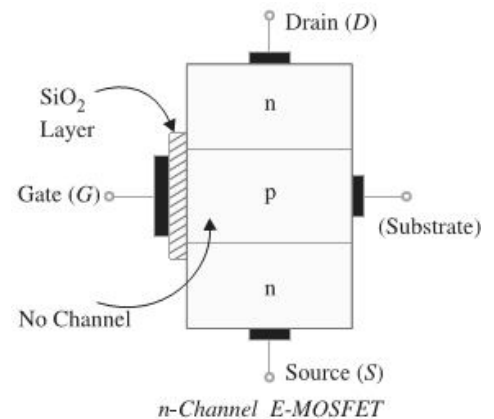
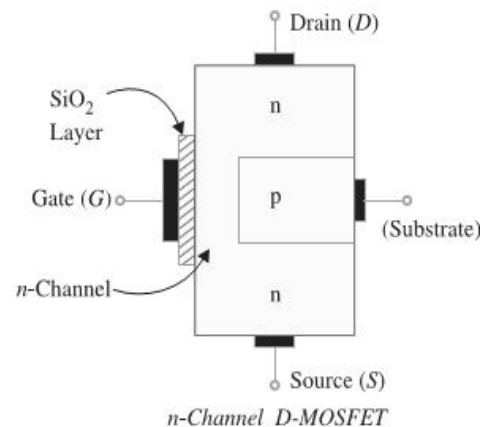➢ Since the gate is insulated from the channel, the MOSFET is sometimes called **insulated-gate FET** (IGFET). However, this term is rarely used in place of the term MOSFET.

❖ **Symbols for D-MOSFET**

There are two types of D-MOSFETs such as

  (i) n-channel D-MOSFET and **(ii)** p-channel D-MOSFET

➢ **(i) N-Channel D-MOSFET**. Fig (i) shows the various parts of n-channel D-MOSFET.


n-Channel D-MOSFET
(i)

➤ The p-type substrate constricts the channel between the source and drain so that only a small passage remains at the left side.

➤ Electrons flowing from source (when drain is positive w.r.t. source) must pass through this narrow channel.

➤ The symbol for n-channel D-MOSFET is shown in Fig (ii).

➤ The gate appears like a capacitor plate. Just to the right of the gate is a thick vertical line representing the channel.

➤ The drain lead comes out of the top of the channel and the source lead connects to the bottom.

➤ The arrow is on the substrate and points to the n-material; therefore we have n-channel D-MOSFET.

➤ It is a usual practice to connect substrate to source internally as shown in Fig. (iii).

➤ This gives rise to a three-terminal device.

➤ **(ii) P-Channel D-MOSFET.** Fig (i) shows the various parts of p-channel D-MOSFET.

➤ The n-type substrate constricts the channel between the source and drain so that only a small passage remains at the left side.

➤ The conduction takes place by the flow of holes from source to drain through this narrow channel.

➤ The symbol for p-channel D-MOSFET shown in Fig (ii). It is a usual practice to connect the substrate to source internally.

➤ This results in a three-terminal device schematic symbol is shown in Fig(iii).
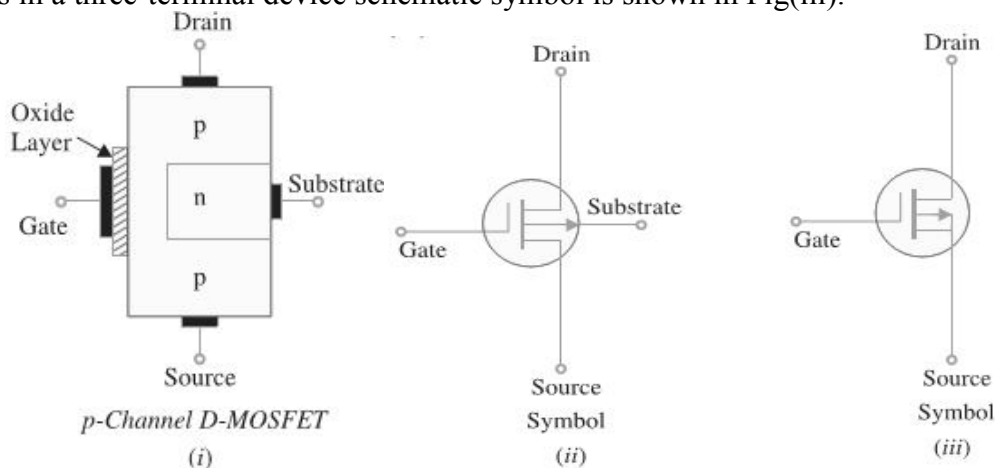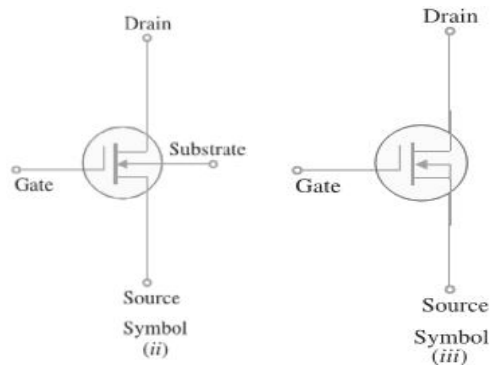
❖ **Circuit Operation of D-MOSFET**

➤ Fig (i) shows the circuit of n-channel D-MOSFET. The gate forms a small capacitor. One plate of this capacitor is the gate and the other plate is the channel with metal oxide layer as the dielectric.

➤ When gate voltage is changed, the electric field of the capacitor changes which in turn changes the resistance of the n-channel.

➤ Since the gate is insulated from the channel, we can apply either negative or positive voltage to the gate.

➤ The negative-gate operation is called **Depletion Mode** whereas positive gate operation is known as **Enhancement Mode**.

♣ **Depletion Mode**. Fig (i) shows depletion-mode operation of n-channel D-MOSFET. Since gate is negative, it means electrons are on the gate as shown is Fig (ii).

➤ These electrons repel the free electrons in the n-channel, leaving a layer of positive ions in a part of the channel as shown in Fig (ii).

➤ In other words, we have depleted (i.e. emptied) the n-channel of some of its free electrons. Therefore, lesser number of free electrons are made available for current conduction through the n- channel.
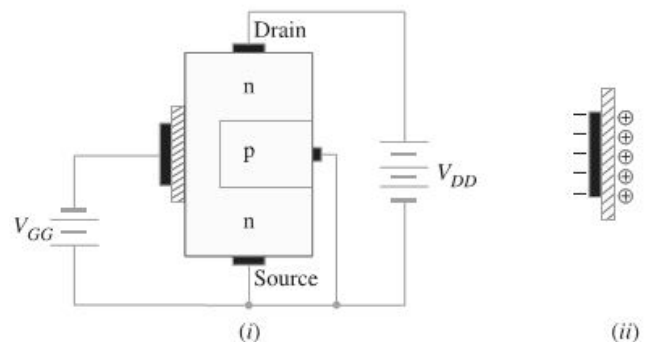
➤ This is the same thing as if the resistance of the channel is increased. The greater the negative voltage on the gate, the lesser is the current from source to drain.

➤ Thus by changing the negative voltage on the gate, we can vary the resistance of the n-channel and hence the current from source to drain.

➤ Note that with negative voltage to the gate, the action of D-MOSFET is similar to JFET.

➤ Because the action with negative gate depends upon depleting (i.e. emptying) the channel of free electrons, the negative-gate operation is called depletion mode.

♣ **(ii) Enhancement Mode.** Fig (i) shows enhancement-mode operation of n-channel D-MOSFET. Again, the gate acts like a capacitor.

➤ Since the gate is positive, it induces negative charges in the n-channel as shown in Fig (ii).

➤ These negative charges are the free electrons drawn into the channel.

➤ Because these free electrons are added to those already in the channel, the total number of free electrons in the channel is increased.

➤ Thus a positive gate voltage enhances or increases the conductivity of the channel.

➤ The greater the positive voltage on the gate, greater the conduction from source to drain.

➤ Thus by changing the positive voltage on the gate, we can change the conductivity of the channel.

➤ The main difference between D-MOSFET and JFET is that we can apply positive gate voltage to D-MOSFET and still have essentially zero current.

➤ Because the action with a positive gate depends upon enhancing the conductivity of the channel, the positive gate operation is called enhancement mode.
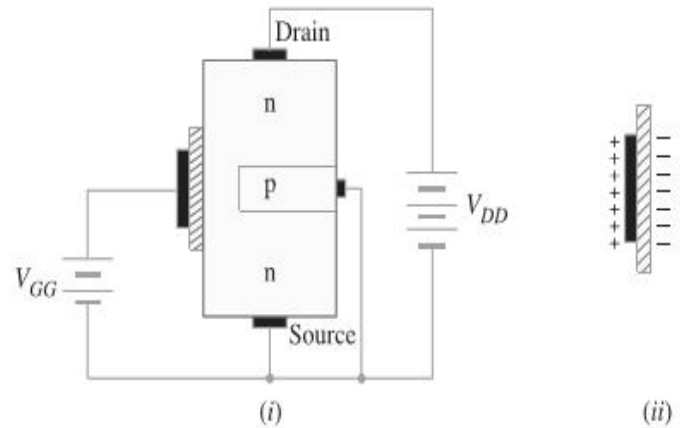
♣ **The following points may be noted about D-MOSFET operation: -**

➤ **(i)** In D-MOSFET, source to drain current is controlled by electric field of capacitor formed at the gate.

➤ **(ii)** The gate of JFET behaves as a reverse-biased diode whereas the gate of a D-MOSFET acts like a capacitor. For this reason, it is possible to operate D-MOSFET with positive or negative gate voltage.

➤ **(iii)** As the gate of D-MOSFET forms a capacitor, therefore, negligible gate current flows whether positive or negative voltage is applied to the gate.

➤ For this, the input impedance of D-MOSFET is very high, ranging from 10,000 MΩ to 10, 000, 00 MΩ.

➤ **(iv)** The extremely small dimensions of the oxide layer under the gate terminal result in a very low capacitance and the D-MOSFET has, therefore, a very low input capacitance.

➤ This characteristic makes the D-MOSFET useful in high-frequency applications.

❖ **D-MOSFET Transfer Characteristic : -**

➤ Fig shows the transfer characteristic curve (or transconductance curve) for n-channel D-OSFET.

➤ The behaviour of this device can be beautifully explained with the help of this curve as under :-

➤ **(i)** The point on the curve where $V_{GS} = 0$, $I_D = I_{DSS}$. It is expected because I_{DSS} is the value of I_D when gate and source terminals are shorted i.e. $V_{GS} = 0$.

➤ **(ii)** As V_{GS} goes negative, I_D decreases below value of I_{DSS} till I_D reaches zero when $V_{GS} = V_{GS(off)}$ just as with JFET.

➤ **(iii)** When V_{GS} is positive, I_D increases above the value of I_{DSS}. The maximum allowable value of I_D is given on the data sheet of D-MOSFET.
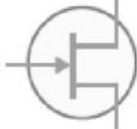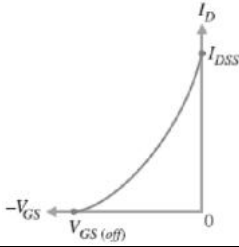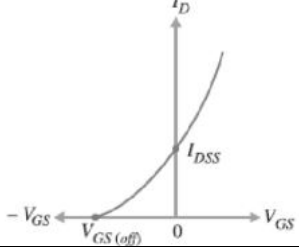
➤ Note that the transconductance curve for the D-MOSFET is very similar to the curve for a JFET.

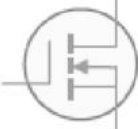➤ Because of this similarity, the JFET and the D-MOSFET have the same transconductance equation viz.
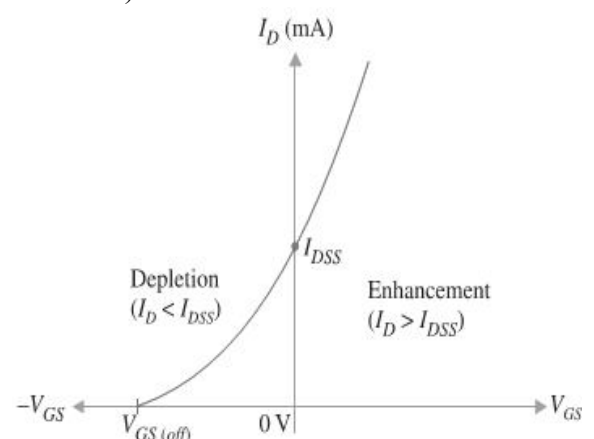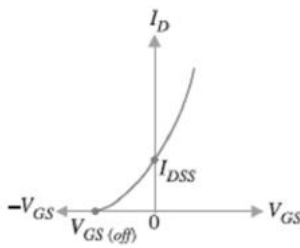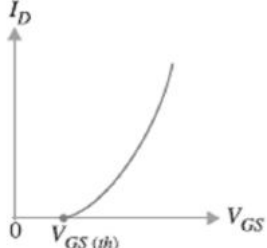
$$\boxed{I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2}$$

❖ **D-MOSFET Vs JFET: -**

SN	Parameters	JFETs	D-MOSFETs
1	Symbol		
2	Transconductance Curve		
3	Modes of operation:	Depletion only	Depletion and enhancement
4	Commonly Used bias circuits:	**(1)** Gate bias; **(2)** Self bias; **(3)** Voltage-divider bias;	**(1)** Gate bias; **(2)** Self bias; **(3)** Voltage-divider bias; **(4)** Zero bias
5	Advantages:	Extremely high input impedance.	**(1)** Higher input impedance than a comparable *JFET*. **(2)** Can operate in both modes (Depletion and Enhancement).
6	Disadvantages:	**(1)**Bias instability; **(2)** Can operate only in depletion mode.	**(1)** Bias instability. **(2)** More sensitive to changes in temperature than the *JFET*.

❖ **Table below summarizes many of the characteristics of D-MOSFETs and E-MOSFETs: -**

SN	Parameters	D-MOSFETs	E-MOSFETs
1	Symbol		
2	Transconductance Curve		
3	Modes of Operation:	Enhancement and Depletion	Enhancement Only
4	Commonly Used bias circuits:	**(1)** Gate bias; **(2)** Self bias; **(3)** Voltage-divider bias; **(4)** Zero bias.	**(1)** Gate bias; **(2)** Voltage-divider bias; **(3)** Drain-feedback bias.

❖ **E-MOSFET: -**

➢ Two things are worth noting about E-MOSFET.
➢ First, E-MOSFET operates only in the enhancement mode and has no depletion mode.
➢ Secondly, the E-MOSFET has no physical channel from source to drain because the substrate extends completely to the SiO_2 layer [See Fig (i)].
➢ It is only by the application of V_{GS} (gate-to-source voltage) of proper magnitude and polarity that the device starts conducting.
➢ The minimum value of V_{GS} of proper polarity that turns on E-MOSFET is called **Threshold voltage** [$V_{GS (th)}$].
➢ The n-channel device requires positive V_{GS} ($\geq V_{GS (th)}$) & the p-channel device requires negative V_{GS} ($\geq V_{GS (th)}$).
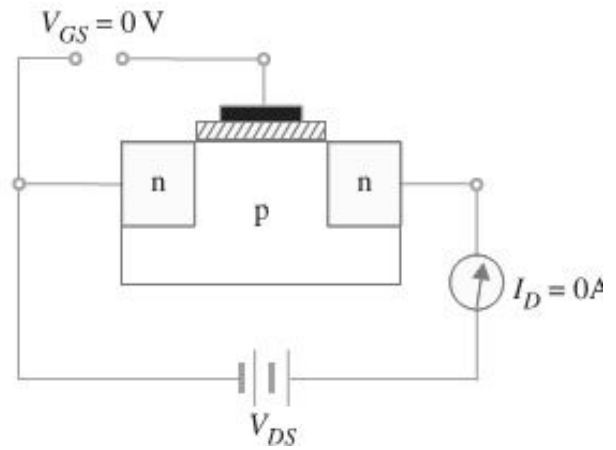
❖ **Power MOSFETs: -**

➢ With the advancement of technology, the engineers have produced a wide variety of MOSEFTs that are designed specifically for high current, high voltage and high power applications.
➢ Some Examples of Power MOSFET are VMOS, LDMOS etc.

❖ **VMOS [V-Grove MOSFET or Vertical MOSFET] :-**

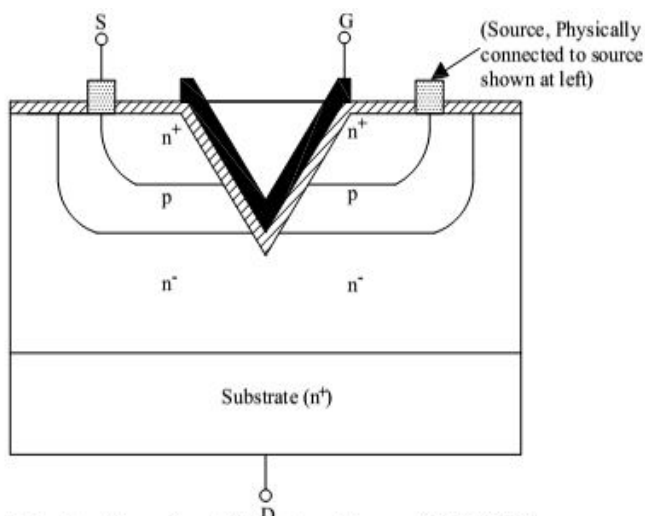➢ One of the major disadvantages of a typical MOSFET is the reduced power handling level as compared to BJT transistors. The power handling level of a typical MOSFET is less than 1W.
➢ This drawback of the MOSFET can be overcome by changing the construction mode from one of the planer nature to one with a vertical structure as shown in Fig.

Illustrating the Construction of VMOS
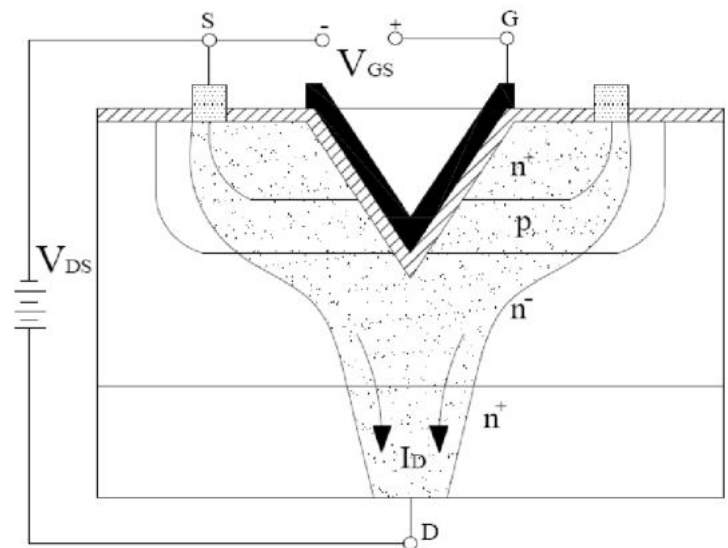
[Illustrating VMOS Operation]

➢ As seen from this figure, all the elements of the planar MOSFET are present in the vertical metal-oxide silicon FET (or simply VMOS) the metallic surface connection to the terminals of the device.
➢ The vertical-MOSEFT (or simple VMOS) is a component designed to handle much larger drain currents than the standard MOSEFT.
➢ The current handling capability of the VMOS is a result of its physical construction which is illustrated in Fig. As seen from this figure, the component gas materials that are labelled as P, N^+ and N^-.
➢ The N^- material labels indicate differences in doping levels.
➢ Also notice that there is no physical channel connecting the source (at top) and the drain (at bottom). Thus VMOS is an *enhancement type* MOSEFT.
➢ With V-shaped gate, a larger channel is formed by a positive gate voltage.
➢ With a large channel, the device is capable of handling large amount of drain current.
➢ The Operation of VMOS is illustrated in Fig.

✚ VMOS Operation: -

➢ When a positive gate voltage is applied to the device, an N-type channel forms in the P-type regions. This effective channel connects the source to the drain.

➢ As seen from the figure the shape of the gate causes a wider channel to form than is created in the standard MOSFET. Hence, the amount of drain current is much higher for this component.

➢ Moreover, the VMOS can exhibit a higher transconductance and a lower turn-on resistance than the conventional planer MOSFET.

➢ Another advantages of using VMOS id the fact it is not susceptible to thermal runaway.

➢ The VMOS has a positive temperature coefficient, means that the resistance of the component increases when temperature increases.

➢ Thus an increase in temperature will cause a decrease in drain current.

➢ The VMOS device can be fabricated with more than one V-grove to increase amount of drain current and some other performance characteristics.

❖ LD MOS: -

➢ The LDMOS (i.e. Lateral Double Diffused MOSFET) is another type of power MOSFET.

➢ This MOSFET uses a very small channel region and a heavily doped N-type region (N^+) to obtain a high drain current and low channel resistance [$r_{d(ON)}$].

➢ Fig shows the basic construction of LDMOS.

➢ As seen from this figure, the narrow channel (Shaded region) is made up of the P-type material that lies between the N^- Substrate (lightly doped) and the N^+ (heavily doped) source region.

➢ Since only the N-type material lies between the channel and the drain, the effective length of the

LDMOS

channel is externally short. This coupled with the N-type material in channel-to-drain path provides an extremely low value of $r_{d\ (ON)}$.

➢ With a low channel resistance, the LDMOS device can handle very high amount of current without generating and damaging amount of heat.

➢ The LDMOS has typical values of $r_{d\ (ON)}$ that are in the range of 2Ω or less.

➢ With this low value channel resistance, it is typically capable of handling current as high as 20 A.
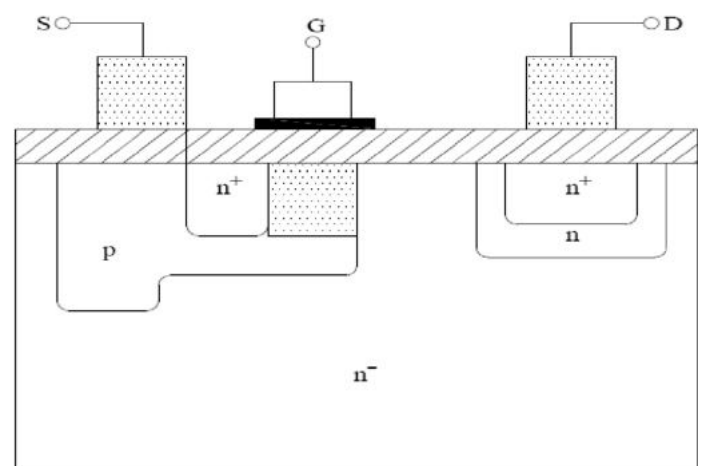
❖ C-MOS: -

➢ C-MOS means complementary MOS. These are mostly used in the field of digital electronics to manufacture logic gates and many other synchronous and asynchronous circuits.

➢ The logic gates includes AND, OR & NOT gates and their various combinations.

➢ The synchronous circuit includes flip-flops, counters, memories, A/D and D/A converters.

➢ The asynchronous circuit includes combinations of logic gates such as decoders, encoders, multiplexers and de-multiplexers etc.

➢ A CMOS logic circuit consists of combinations of NMOS & PMOS devices.

[CHAPTER-5]

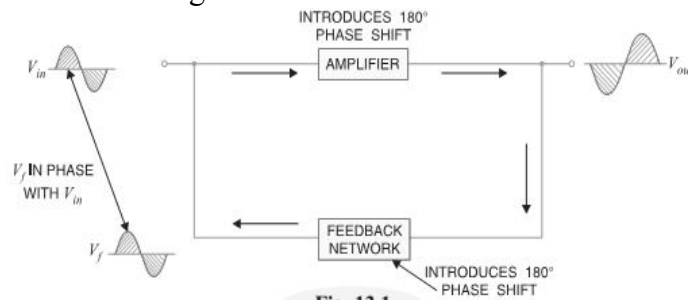-------------------------------- [FEED BACK AMPLIFIER] --------------------------------

❖ **INTRODUCTION:-**

✍ A practical amplifier has a gain of nearly one million i.e. its output is one million times the input. Consequently, even a casual disturbance at the input will appear in the amplified form in the output.

✍ The noise in the output of an amplifier is undesirable and must be kept to as small a level as possible. The noise level in amplifiers can be reduced considerably by the use of negative feedback i.e. by injecting a fraction of output in phase opposition to the input signal.

✍ The object of this chapter is to consider the effects and methods of providing negative feedback in transistor amplifiers.

❖ **FEEDBACK:-**

✍ The process of injecting a fraction of output energy of some device back to the input is known as **feedback.** Depending upon whether the feedback energy aids or opposes the input signal, there are two basic types of feedback in amplifiers viz Positive Feedback and Negative Feedback.

✚ **Positive Feedback**. When the feedback energy (voltage or current) is in phase with the input signal and thus aids it, it is called *positive feedback*. This is illustrated in Fig.
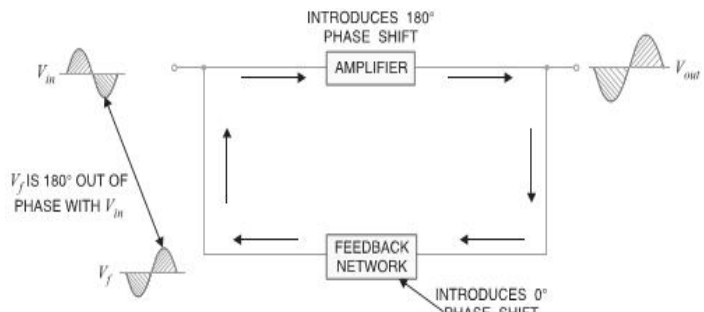
✍ Both amplifier and feedback network introduce a phase shift of 180°. The result is a 360° phase shift around the loop, causing the feedback voltage V_f to be in phase with the input signal V_{in}.

✍ The positive feedback increases the gain of the amplifier. However, it has the disadvantages of increased distortion and instability. Therefore, positive feedback is not often employed in amplifiers.

✍ One important use of positive feedback is in oscillators. If positive feedback is sufficiently large, it leads to oscillations. As a matter of fact, an oscillator is a device that converts d.c. power into a.c. power of any desired frequency.

✚ **(ii) Negative Feedback.** When the feedback energy (voltage or current) is out of phase with the input signal and thus opposes it, it is called *negative feedback*. This is illustrated in Fig.

✍ As you can see, the amplifier introduces a phase shift of 180° into the circuit while the feedback network is so designed that it introduces no phase shift (i.e., 0° phase shift). The result is that the feedback voltage V_f is 180° out of phase with the input signal V_{in}.

✍ Negative feedback reduces the gain of the amplifier. However, the advantages of negative feedback are: reduction in distortion, stability in gain, increased bandwidth and improved input and output impedances.

✍ It is due to these advantages that negative feedback is frequently employed in amplifiers.

❖ **PRINCIPLES OF NEGATIVE VOLTAGE FEEDBACK IN AMPLIFIERS:-**

✍ A feedback amplifier has main two parts such as an amplifier and a feedback circuit.

✍ The feedback circuit usually consists of resistors and returns a fraction of output energy back to the input.

✍ Fig. shows the principles of negative voltage feedback in an amplifier. Typical values have been assumed to make the treatment more illustrative.

✍ The output of the amplifier is 10 V. The fraction m_v of this output i.e.100 mV is feedback to the input where it is applied in series with the input signal of 101 mV.

✍ As the feedback is negative, therefore, only 1 mV appears at the input terminals of the amplifier.
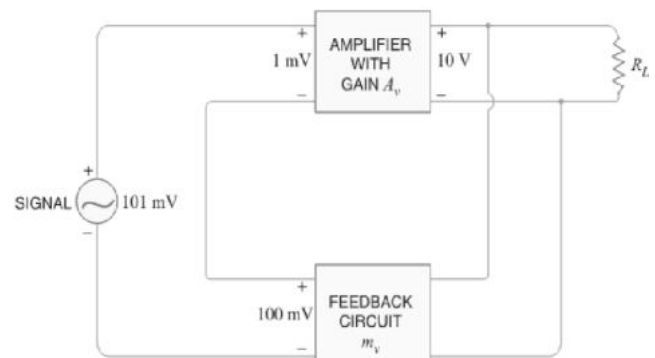
- ✎ Referring to Fig., we have,
  - ♣ Gain of amplifier without feedback, $A_v = (10\ V)/(1\ mV) = 10{,}000$
  - ♣ Fraction of output voltage feedback, $m_v = (100\ mV)/10V = 0.01$
  - ♣ Gain of amplifier with negative feedback, $A_{vf} = 10V/101mV = 100$

- ✎ The following points are worth noting:-
- ♣ When negative voltage feedback is applied, the gain of the amplifier is reduced. Thus, the gain of above amplifier without feedback is 10,000 whereas with negative feedback, it is only 100.
- ♣ When negative voltage feedback is employed, the voltage actually applied to the amplifier is extremely small. In this case, the signal voltage is 101 mV and the negative feedback is 100 mV so that voltage applied at the input of the amplifier is only 1 mV.
- ♣ In a negative voltage feedback circuit, the feedback fraction m_v is always between 0 and 1.
- ♣ The gain with feedback is sometimes called **closed-loop gain** while the gain without feedback is called *open-loop gain*. These terms come from the fact that amplifier and feedback circuits form a "loop".
- ♣ When loop is "opened" by disconnecting feedback circuit from I/P, amplifier's gain A_v ,[open-loop gain]
- ♣ When the loop is "closed" by connecting the feedback circuit, gain decreases to A_{vf} ["closed-loop" gain]

❖ GAIN OF NEGATIVE VOLTAGE FEEDBACK AMPLIFIER:-

- ✎ Consider the negative voltage feedback amplifier shown in Fig.
- ✎ The gain of the amplifier without feedback is A_v.
- ✎ Negative feedback is then applied by feeding a fraction m_v of the output voltage e_0 back to amplifier input.
- ✎ Therefore, the actual input to the amplifier is the signal voltage e_g minus feedback voltage $m_v\,e_0$ i.e.,

  Actual input to amplifier $= (e_g - m_v e_0)$
  The output e_0 must be equal to the input voltage
  $(e_g - m_v e_0)$ multiplied by gain A_v of the amplifier   i.e.

  $(e_g - m_v e_0)\,A_v = e_0$ ➔ $A_v e_g - A_v\,m_v\,e_0 = e_0$

  ➔ $e_0 + A_v\,m_v\,e_0 = A_v e_g$ ➔ $e_0(1 + A_v\,m_v) = A_v e_g$

$$\frac{e_0}{e_g} = \frac{A_v}{1 + A_v m_v}$$

- ✎ But e_0/e_g is the voltage gain of the amplifier with feedback.
  ∴   Voltage gain with negative feedback is

$$A_{vf} = \frac{A_v}{1 + A_v m_v}$$

- ✎ It may be seen that the gain of the amplifier without feedback is A_v. However, when negative voltage feedback is applied, the gain is reduced by a factor $1 + A_v\,m_v$.
- ✎ It may be noted that negative voltage feedback does not affect the current gain of the circuit.

❖ ADVANTAGES OF NEGATIVE VOLTAGE FEEDBACK:-

- ✎ The following are the advantages of negative voltage feedback in amplifiers:-
- ♣ **Gain Stability**. An important advantage of negative voltage feedback is that the resultant gain of the amplifier can be made independent of transistor parameters or the supply voltage variations.

$$A_{vf} = \frac{A_v}{1 + A_v\,m_v}$$

- ✎ For negative voltage feedback in an amplifier to be effective, the designer deliberately makes the product $A_v m_v$ much greater than unity. Therefore, in the above relation, 1 can be neglected as compared to $A_v m_v$ and the expression becomes:

$$A_{vf} = \frac{A_v}{A_v\,m_v} = \frac{1}{m_v}$$

- ✎ It may be seen that the gain now depends only upon feedback fraction m_v i.e., on the characteristics of feedback circuit. As feedback circuit is usually a voltage divider (a resistive network), therefore, it is unaffected by changes in temperature, variations in transistor parameters and frequency. Hence, the gain of the amplifier is extremely stable.

♣ **(ii) Reduces non-linear Distortion.** A large signal stage has non-linear distortion because its voltage gain changes at various points in the cycle. The negative voltage feedback reduces the nonlinear distortion in large signal amplifiers. It can be proved mathematically that:

$$D_{vf} = \frac{D}{1 + A_v \, m_v}$$

Where D = distortion in amplifier without feedback

 D_{vf} = distortion in amplifier with negative feedback

✎ Thus by applying negative voltage feedback to an amplifier, distortion is reduced by a factor $1 + A_v \, m_v$.

♣ **(iii)Improves Frequency Response**. As feedback is usually obtained through a resistive network, therefore, voltage gain of the amplifier is independent of signal frequency. The result is that voltage gain of the amplifier will be substantially constant over a wide range of signal frequency. The negative voltage feedback, therefore, improves the frequency response of the amplifier.

♣ **(iv)Increases Circuit Stability.** The output of an ordinary amplifier is easily changed due to variations in ambient temperature, frequency and signal amplitude. This changes the gain of the amplifier, resulting in distortion. However, by applying negative voltage feedback, voltage gain of the amplifier is stabilized or accurately fixed in value. This can be easily explained. Suppose the output of a negative voltage feedback amplifier has increased because of temperature change or due to some other reason. This means more negative feedback since feedback is being given from the output. This tends to oppose the increase in amplification and maintains it stable. The same is true should the output voltage decrease. Consequently, the circuit stability is considerably increased.

♣ **(v) Increases input impedance and decreases output impedance.** The negative voltage feedback increases the input impedance and decreases the output impedance of amplifier. Such a change is profitable in practice as the amplifier can then serve the purpose of impedance matching.

❖ **FEEDBACK CIRCUIT:-**

✎ The function of the feedback circuit is to return a fraction of the output voltage to the input of the amplifier.

✎ Fig. shows the feedback circuit of negative voltage feedback amplifier. It is essentially a potential divider consisting of resistances R_1 and R_2.

✎ The output voltage of the amplifier is fed to this potential divider which gives the feedback voltage to the input.

✎ Referring to Fig. it is clear that :

Voltage across $R_1 = \left(\frac{R_1}{R_1 + R_2}\right) e_0$

Feedback fraction, $m_v = \frac{Voltage \; across \; R_1}{e_0} = \frac{R_1}{R_1 + R_2}$
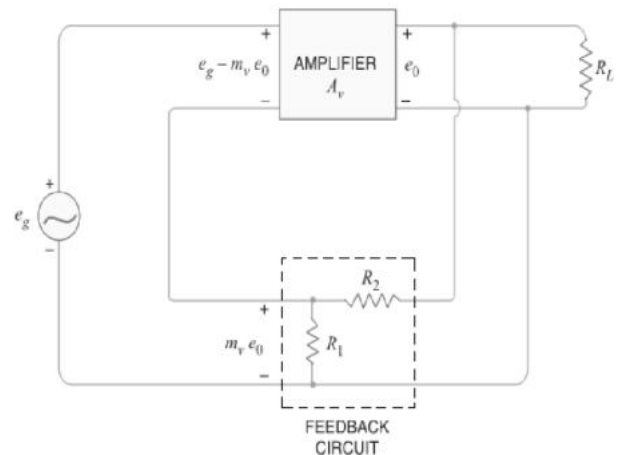
❖ **INPUT & OUTPUT IMPEDANCE OF NEGATIVE FEEDBACK AMPLIFIER :-**

♣ **(a) Input impedance.** The increase in input impedance with negative voltage feedback can be explained by referring to Fig. Suppose the input impedance of the amplifier is Z_{in} without feedback and Z'_{in} with negative feedback. Let us further assume that input current is i_1.

✎ Referring to Fig., we have,

$e_g - m_v e_0 = i_1 Z_{in}$

Now $e_g = (e_g - m_v \, e_0) + m_v \, e_0$

         $= (e_g - m_v e_0) + A_v \, m_v \, (e_g - m_v e_0)$

                 $[\because e_0 = A_v \, (e_g - m_v e_0)]$

         $= (e_g - m_v e_0) \, (1 + A_v m_v)$

         $= i_1 Z_{in} \, (1 + A_v \, m_v)$ $[\because e_g - m_v \, e_0 = i_1 Z_{in}]$

Or $\frac{e_g}{i_1} = Z_{in} \, (1 + A_v \, m_v)$

But $\frac{e_g}{i_1} = Z'_{in}$, the input impedance of the amplifier with negative voltage feedback.

$$\therefore \quad Z'_{in} = Z_{in} \, (1 + A_v \, m_v)$$
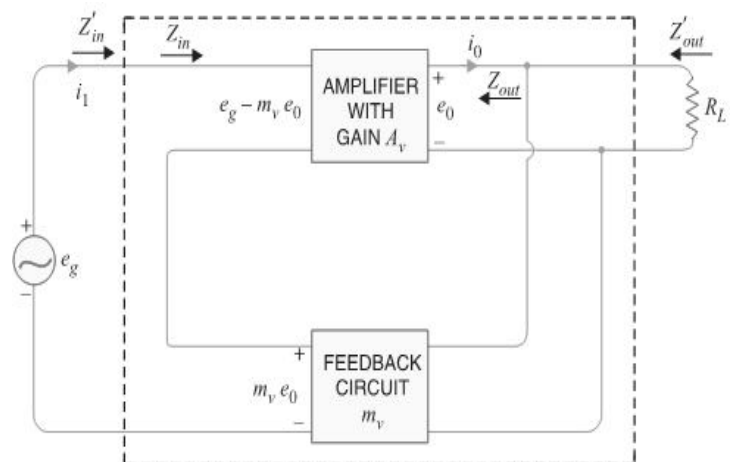
✎ It is clear that by applying negative voltage feedback, the input impedance of the amplifier is increased by a factor $1 + A_v m_v$. As $A_v m_v$ is much greater than unity.

✎ Therefore, input impedance is increased considerably. This is an advantage, since the amplifier will now present less of a load to its source circuit.

♣ **(b) Output impedance.** Following similar line, we can show that output impedance with negative voltage feedback is given by :

$$\therefore \quad Z'_{out} = \frac{Z_{out}}{1 + A_v m_v}$$

Where
Z'_{out} = output impedance with negative voltage feedback
Z_{out} = output impedance without feedback

✎ It is clear that by applying negative feedback, the output impedance of the amplifier is decreased by a factor $1 + A_v m_v$.

✎ This is an added benefit of using negative voltage feedback.

✎ With lower value of output impedance, the amplifier is much better suited to drive low impedance loads.

❖ **EMITTER FOLLOWER:-**

✎ It is a negative current feedback circuit. The emitter follower is a current amplifier that has no voltage gain. Its most important characteristic is that it has high input impedance and low output impedance.

✎ This makes it an ideal circuit for impedance matching.

♣ **Circuit Details.**

✎ Fig. shows the circuit of an emitter follower. As we can see, it differs from the circuitry of a conventional CE amplifier by the absence of *collector load* and *emitter bypass capacitor*.

✎ The emitter resistance R_E itself acts as the load and a.c. output voltage (V_{out}) is taken across R_E.

✎ The biasing is generally provided by voltage-divider method or by base resistor method.

✎ The following points are worth noting about the emitter follower:
  (i) There is neither collector resistor in the circuit nor there is emitter bypass capacitor.
  (ii) These are the two circuit recognition features of the emitter follower.
  (iii) Since the collector is at ac ground, this circuit is also known as common collector (CC) amplifier.

♣ **Operation.** The input voltage is applied between base and emitter and the resulting a.c. emitter current produces an output voltage $i_e R_E$ across the emitter resistance.

✎ This voltage opposes the input voltage, thus providing negative feedback.

✎ Clearly, it is a negative current feedback circuit since the voltage feedback is proportional to the emitter current i.e., output current.

✎ It is called **emitter follower** because the output voltage follows the input voltage.

♣ **Characteristics**.

✎ The major characteristics of the emitter follower are:-
  (i) No voltage gain. In fact, the voltage gain of an emitter follower is close to 1.
  (ii) Relatively high current gain and power gain.
  (iii) High input impedance and low output impedance.
  (iv) Input and output ac voltages are in phase.

♣ **APPLICATIONS**

✎ The emitter follower has the following principal applications:
  (i) To provide current amplification with no voltage gain.
  (ii) Impedance matching.
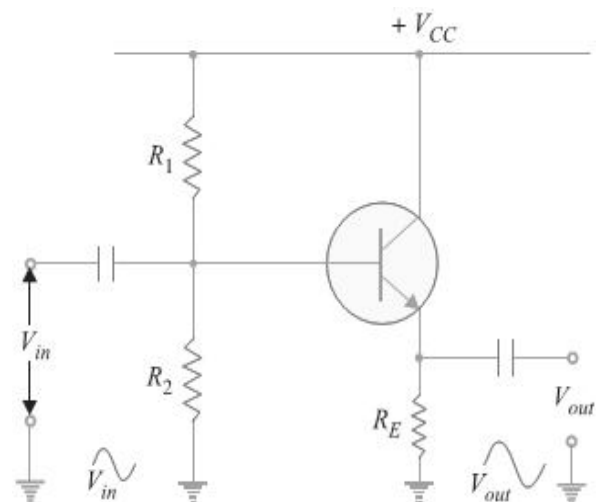
❖ **DARLINGTON AMPLIFIER:-**

✎ Sometimes, the current gain and input impedance of an emitter follower are insufficient to meet the requirement.

✎ In order to increase the overall values of circuit current gain (A_i) and input impedance, two transistors are connected in series in emitter follower configuration as shown in Fig.

✎ Such a circuit is called **Darlington amplifier**.

✎ Note that emitter of first transistor is connected to the base of the second transistor and the collector terminals of the two transistors are connected together.

✎ The result is that emitter current of the first transistor is the base current of the second transistor.

✎ Therefore, the current gain of the pair is equal to product of individual current gains i.e.
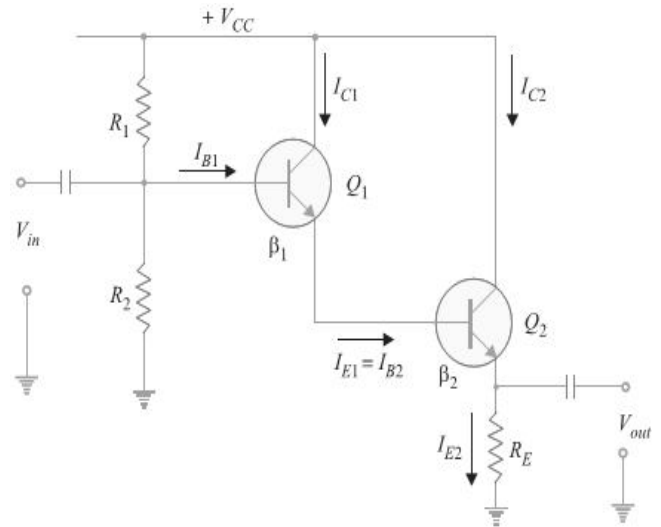
$$\beta = \beta_1\beta_2$$

✎ Note that high current gain is achieved with a minimum use of components. The biasing analysis is similar to that for one transistor except that two V_{BE} drops are to be considered.

✎ Thus referring to Fig.,

Voltage across R_2, $V_2 = \dfrac{V_{CC}}{R_1 + R_2} \times R_2$

Voltage across R_E, $V_E = V_2 - 2V_{BE}$
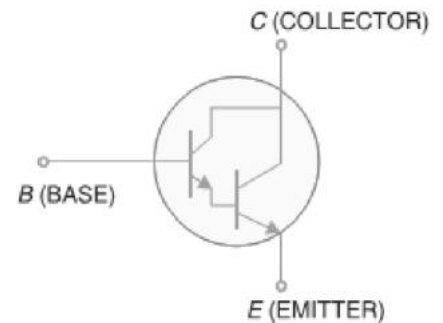
Current through R_E, $I_{E2} = \dfrac{V_2 - 2V_{BE}}{R_E}$

✎ Since the transistors are directly coupled, $I_{E1} = I_{B2}$. Now $I_{B2} = I_{E2}/\beta_2$.

∴ $I_{E1} = \dfrac{I_{E2}}{\beta_2}$

The boxed derivation:

$I_{E1} = \beta_1 I_{B1}$ ($\because I_{E1} \simeq I_{C1}$)

Now I_{E1} is the base current of Q_2 i.e. $I_{E1} = I_{B2}$.

Now $I_{E2} = \beta_2 I_{B2} = \beta_2 I_{E1} = \beta_2 \beta_1 I_{B1}$

∴ Overall current gain, $\beta = \dfrac{I_{E2}}{I_{B1}} = \dfrac{\beta_1 \beta_2 I_{B1}}{I_{B1}} = \beta_1\beta_2$

✎ In practice, the two transistors are put inside single transistor housing and three terminals E, B and C are brought out as shown in Fig.

✎ This three terminal device is known as a **Darlington transistor**.

✎ The Darlington transistor acts like a single transistor that has high current gain and high input impedance.

♣ **Characteristics.** The following are the important characteristics of Darlington amplifier:

(i) Extremely high input impedance (MΩ).
(ii) Extremely high current gain (several thousands).
(iii)Extremely low output impedance (a few Ω).

✎ Since the characteristics of the Darlington amplifier are basically the same as those of the emitter follower, the two circuits are used for similar applications.

✎ When you need higher input impedance and current gain and/or lower output impedance than the standard emitter follower can provide, you use a Darlington amplifier.

✎ Darlington transistors are commonly available. Like standard transistors, they have only three terminals but they have much higher values of current gain and input impedance.

[CHAPTER-6]

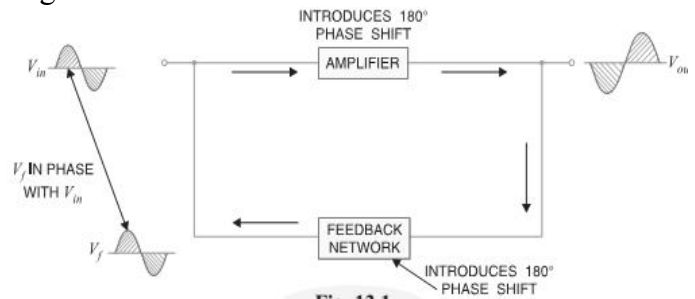-------------------------------- [SINUSOIDAL OSCILLATOR] --------------------------------

❖ **FEEDBACK:-**

✎ The process of injecting a fraction of output energy of some device back to the input is known as feedback.

✎ Depending upon whether the feedback energy aids or opposes the input signal, there are two basic types of feedback in amplifiers viz Positive Feedback and Negative Feedback.

♦ **Positive Feedback**. When the feedback energy (voltage or current) is in phase with the input signal and thus aids it, it is called *positive feedback*. This is illustrated in Fig.
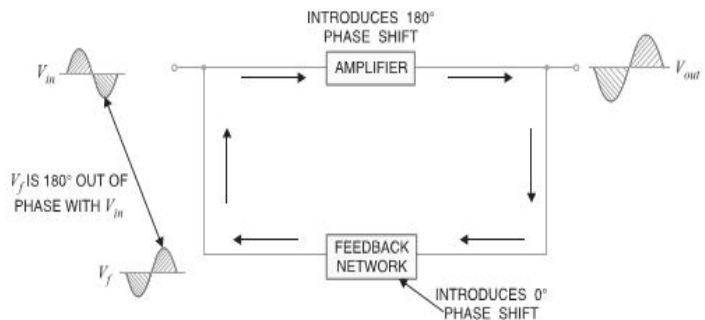
✎ Both amplifier and feedback network introduce a phase shift of 180°. The result is a 360° phase shift around the loop, causing the feedback voltage V_f to be in phase with the input signal V_{in}.

✎ The positive feedback increases the gain of the amplifier. However, it has the disadvantages of increased distortion and instability. Therefore, positive feedback is not often employed in amplifiers.

✎ One important use of positive feedback is in oscillators. If positive feedback is sufficiently large, it leads to oscillations. As a matter of fact, an oscillator is a device that converts d.c. power into a.c. power of any desired frequency.

♦ **(ii) Negative Feedback.** When the feedback energy (voltage or current) is out of phase with the input signal and thus opposes it, it is called *negative feedback*. This is illustrated in Fig.

✎ As you can see, the amplifier introduces a phase shift of 180° into the circuit while the feedback network is so designed that it introduces no phase shift (i.e., 0° phase shift). The result is that the feedback voltage V_f is 180° out of phase with the input signal V_{in}.

✎ Negative feedback reduces the gain of the amplifier. However, the advantages of negative feedback are: reduction in distortion, stability in gain, increased bandwidth and improved input and output impedances.

❖ It is due to these advantages that negative feedback is frequently employed in amplifiers.

❖ **Types Of Feedback Connections: -**

✎ There are four basic types of connecting the feedback signal from an amplifier output to its input : -

- ♣ Voltage-Series feedback connection.
- ♣ Voltage-Shunt feedback connection.
- ♣ Current-Series feedback connection.
- ♣ Current-Shunt feedback connection.

✎ It means that both voltage and current can be feedback to the input either in series or parallel.

✎ In the feedback connection types, the term **'voltage'** refers to connecting the output voltage as input to the feedback network.

✎ The term **'current'** refers to tapping off some output current through the feedback network.

✎ The term '**series**' refers to connecting the feedback signal in series with the input signal voltage.

✎ The term '**shunt'** refers to connecting the feedback signal in shunt (parallel) with an input current source.

✎ It has been observed that the series feedback connections tend to increase the input resistance, while the shunt feedback connection tends to decrease the input resistance.

✎ Moreover, the voltage feedback will tend to decrease the output resistance.

✎ As a matter of fact, higher input resistance and lower output resistance is desired for most cascade amplifiers.

✎ Both of these characteristic are obtained by using the voltage – series feedback connection.
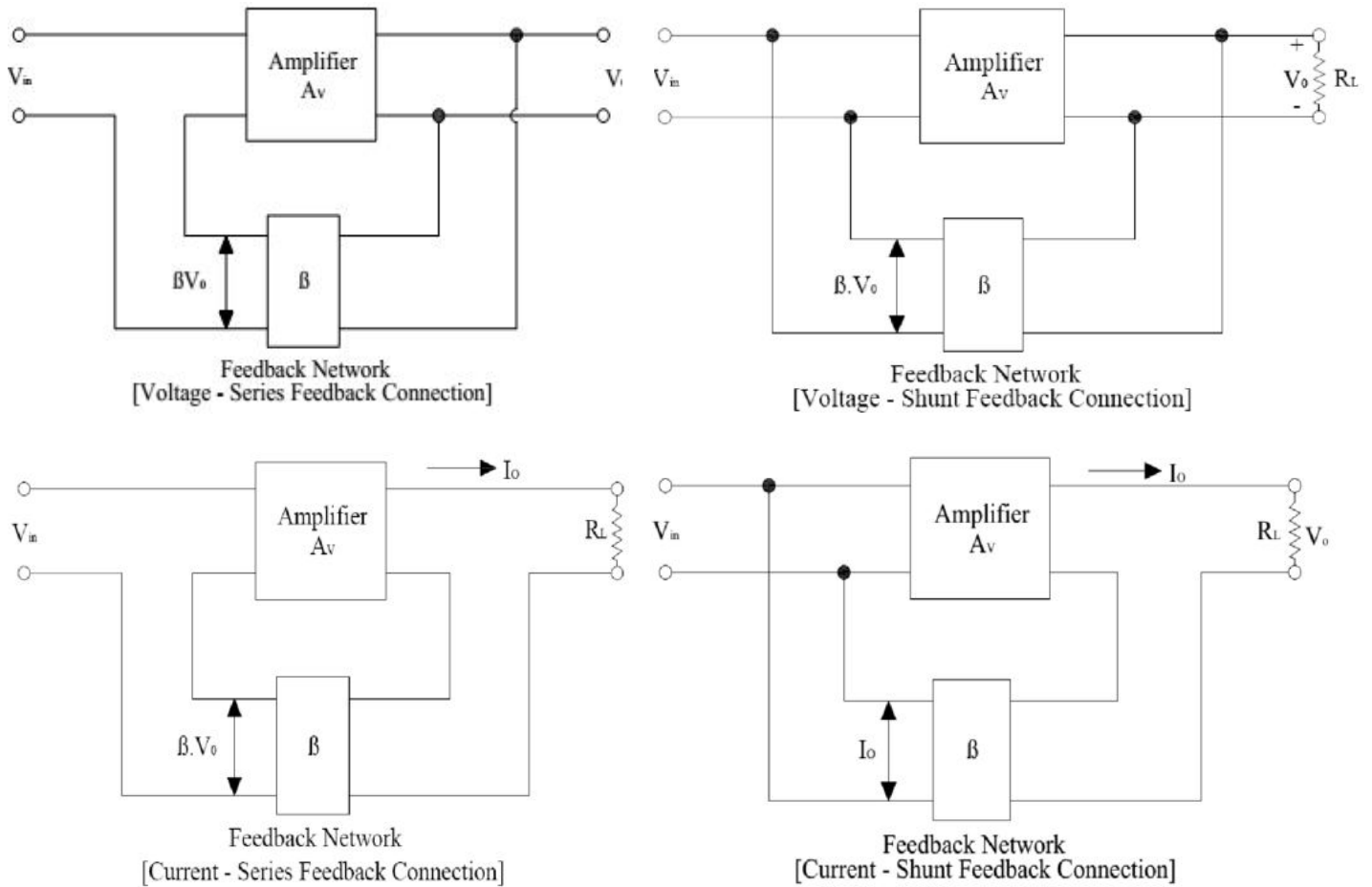
Feedback Network
[Voltage - Series Feedback Connection]

Feedback Network
[Voltage - Shunt Feedback Connection]

Feedback Network
[Current - Series Feedback Connection]

Feedback Network
[Current - Shunt Feedback Connection]

❖ ADVANTAGES OF NEGATIVE VOLTAGE FEEDBACK:-

✎ The following are the advantages of negative voltage feedback in amplifiers:-

♣ **(i) Gain Stability**. An important advantage of negative voltage feedback is that the resultant gain of the amplifier can be made independent of transistor parameters or the supply voltage variations.

$$A_{vf} = \frac{A_v}{1 + A_v \, m_v}$$

✎ For negative voltage feedback in an amplifier to be effective, the designer deliberately makes the product $A_v m_v$ much greater than unity. Therefore, in the above relation, 1 can be neglected as compared to $A_v m_v$ and the expression becomes:

$$A_{vf} = \frac{A_v}{A_v \, m_v} = \frac{1}{m_v}$$

✎ It may be seen that the gain now depends only upon feedback fraction m_v i.e., on the characteristics of feedback circuit. As feedback circuit is usually a voltage divider (a resistive network), therefore, it is unaffected by changes in temperature, variations in transistor parameters and frequency. Hence, the gain of the amplifier is extremely stable.

♣ **(ii) Reduces non-linear Distortion.** A large signal stage has non-linear distortion because its voltage gain changes at various points in the cycle. The negative voltage feedback reduces the nonlinear distortion in large signal amplifiers. It can be proved mathematically that:

$$D_{vf} = \frac{D}{1 + A_v \, m_v}$$

Where   D = distortion in amplifier without feedback

                                    D_{vf} = distortion in amplifier with negative feedback

✎ Thus by applying negative voltage feedback to an amplifier, distortion is reduced by a factor $1 + A_v \, m_v$.

♣ **(iii)Improves Frequency Response**. As feedback is usually obtained through a resistive network, therefore, voltage gain of the amplifier is independent of signal frequency.

✎ The result is that voltage gain of the amplifier will be substantially constant over a wide range of signal frequency. The negative voltage feedback, therefore, improves the frequency response of the amplifier.

♣ **(iv)Increases Circuit Stability.** The output of an ordinary amplifier is easily changed due to variations in ambient temperature, frequency and signal amplitude.

✍ This changes the gain of the amplifier, resulting in distortion. However, by applying negative voltage feedback, voltage gain of the amplifier is stabilized or accurately fixed in value.

✍ This can be easily explained. Suppose the output of a negative voltage feedback amplifier has increased because of temperature change or due to some other reason.

✍ This means more negative feedback since feedback is being given from the output. This tends to oppose the increase in amplification and maintains it stable. The same is true should the output voltage decrease. Consequently, the circuit stability is considerably increased.

✍ **(v) Increases input impedance and decreases output impedance.** The negative voltage feedback increases the input impedance and decreases the output impedance of amplifier. Such a change is profitable in practice as the amplifier can then serve the purpose of impedance matching.

❖ **INTRODUCTION TO OSCILLATOR,**

✍ Many electronic devices require a source of energy at a specific frequency which may range from a few Hz to several MHz. This is achieved by an electronic device called an oscillator.

✍ Oscillators are extensively used in electronic equipment. For example, in radio and television receivers, oscillators are used to generate high frequency wave (called carrier wave) in the tuning stages.

✍ Audio frequency and radiofrequency signals are required for the repair of radio, television and other electronic equipment. Oscillators are also widely used in radar, electronic computers and other electronic devices. Oscillators can produce sinusoidal or non-sinusoidal (e.g. square wave) waves.

❖ **SINUSOIDAL OSCILLATORS:-**

✍ An electronic device that generates sinusoidal oscillations of desired frequency is known as a **sinusoidal oscillator**. Although we speak of an oscillator as "generating" a frequency, it should be noted that it does not create energy, but merely acts as an energy converter.

✍ It receives D.C. energy and changes it into A.C. energy of our desired frequency.

✍ The frequency of oscillations depends upon the constants of the device. It may be mentioned here that although an alternator produces sinusoidal oscillations of 50Hz, it cannot be called an oscillator.

✍ **Firstly**, An alternator is a mechanical device having rotating parts whereas an oscillator is a non-rotating electronic device. **Secondly**, An alternator converts Mechanical Energy into A.C. Energy while an oscillator converts D.C. Energy into A.C. energy. **Thirdly**, An alternator cannot produce high frequency oscillations whereas an oscillator can produce oscillations ranging from a few Hz to several MHz.

❖ **ADVANTAGES**

✍ Although oscillations can be produced by mechanical devices (e.g. alternators), but electronic oscillators have the following advantages:

♣ An oscillator is a non-rotating device. Consequently, there is little wear and tear and hence longer life.

♣ Due to the absence of moving parts, the operation of an oscillator is quite silent.

♣ An oscillator can produce waves from small (20 Hz) to extremely high frequencies (> 100 MHz).

♣ The frequency of oscillations can be easily changed when desired.

♣ It has good frequency stability i.e. frequency once set remains constant for a considerable period of time.

♣ It has very high efficiency.

❖ **TYPES OF SINUSOIDAL OSCILLATIONS:-**

✍ Sinusoidal oscillations can be of two types viz **Damped Oscillations** and **Undamped Oscillations**.

♣ **(i) Damped Oscillations**: - The electrical oscillations whose amplitude goes on decreasing with time are called damped oscillations. Fig (i) Shows waveform of damped electrical oscillations.

✍ Obviously, the electrical system in which these oscillations are generated has losses and some energy is lost during each oscillation.

✍ Further, no means are provided to compensate for the losses and consequently the amplitude of the generated wave decreases gradually. It may be noted that frequency of oscillations remains unchanged since it depends upon the constants of the electrical system.

(i)   (ii)
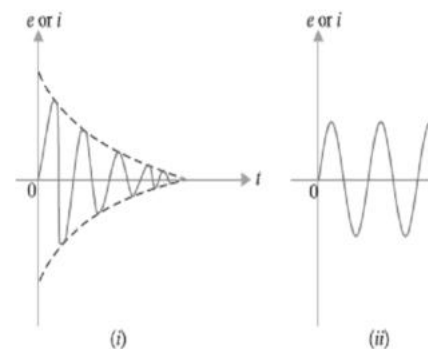
♣ **(ii) Undamped Oscillations**. The electrical oscillations whose amplitude remains constant with time are called undamped oscillations. Fig. (ii) Shows waveform of undamped electrical oscillations.

(ii)

🖎 Although the electrical system in which these oscillations are being generated has also losses, but now right amount of energy is being supplied to overcome the losses.

🖎 Consequently, the amplitude of the generated wave remains constant. It should be emphasized that an oscillator is required to produce undamped electrical oscillations for utilizing in various electronics equipment.
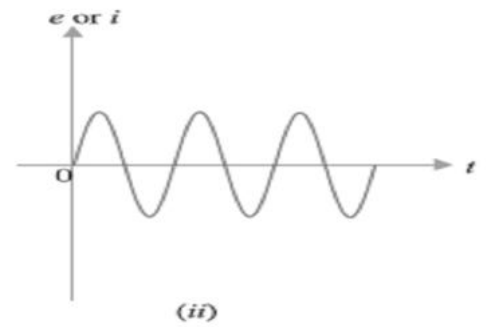
❖ **OSCILLATORY CIRCUIT: -**

🖎 A circuit which produces electrical oscillations of any desired frequency is known as an **Oscillatory Circuit** or **Tank Circuit**.

🖎 A simple oscillatory circuit consists of a capacitor (C) and inductance coil (L) in parallel as shown in Fig. This system can produce electrical oscillations of frequency determined by the values of L and C.

🖎 To understand how this comes about, suppose the capacitor is charged from a d.c. source with a polarity as shown in Fig. (i).

(i)   *(ii)*   *(iii)*   *(iv)*
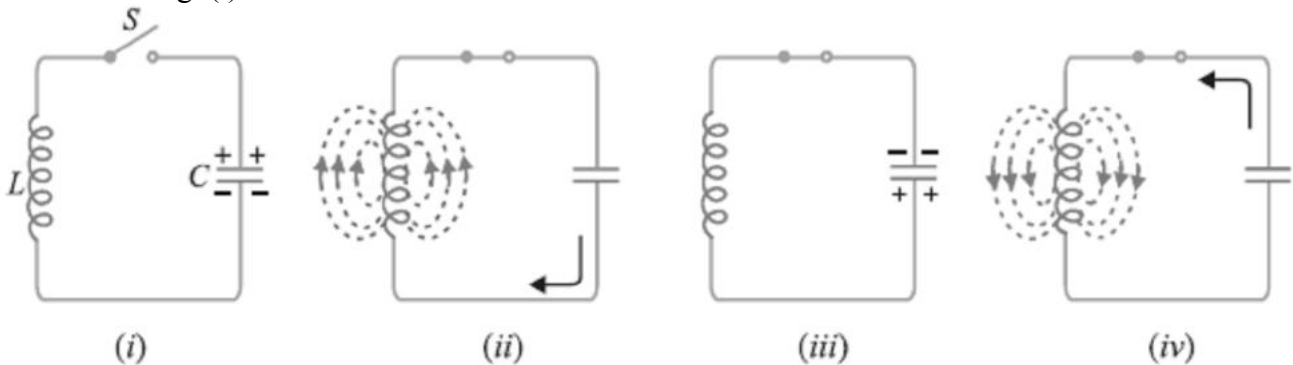
🖎 **(i)** In the position shown in Fig (i), the upper plate of capacitor has deficit of electrons and the lower plate has excess of electrons. Therefore, there is a voltage across the capacitor and the capacitor has electrostatic energy.

🖎 **(ii)** When switch Sis closed as shown in Fig (ii), the capacitor will discharge through inductance and the electron flow will be in the direction indicated by the arrow.

🖎 This current flow sets up magnetic field around the coil. Due to the inductive effect, the current builds up slowly towards a maximum value.

🖎 The circuit current will be maximum when the capacitor is fully discharged. At this instant, electrostatic energy is zero but because electron motion is greatest (i.e. maximum current), the magnetic field energy around the coil is maximum. This is shown in Fig (ii).

🖎 Obviously, the electrostatic energy across the capacitor is completely converted into magnetic field energy around the coil.

🖎 **(iii)** Once the capacitor is discharged, the magnetic field will begin to collapse and produce a counter e.m.f. According to Lenz's law, the counter e.m.f. will keep the current flowing in the same direction.

🖎 The result is that the capacitor is now charged with opposite polarity, making upper plate of capacitor negative and lower plate positive as shown in Fig (iii).

🖎 **(iv)** After the collapsing field has recharged the capacitor, the capacitor now begins to discharge; current now flowing in the opposite direction.

🖎 Fig (iv) shows capacitor fully discharged and maximum current flowing. The sequence of charge and discharge results in alternating motion of electrons or an oscillating current.

🖎 The energy is alternately stored in the electric field of the capacitor (C) and the magnetic field of the inductance coil (L). This interchange of energy between L and C is repeated over and again resulting in the production of oscillations.

♣ **WAVEFORM.**

✎ If there were no losses in the tank circuit to consume the energy, the interchange of energy between L and C would continue indefinitely.

✎ In a practical tank circuit, there are resistive and radiation losses in the coil and dielectric losses in the capacitor. During each cycle, a small part of the originally imparted energy is used up to overcome these losses.

✎ The result is that the amplitude of oscillating current decreases gradually and eventually it becomes zero when all the energy is consumed as losses.

✎ Therefore, the tank circuit by itself will produce damped oscillations as shown in Fig.
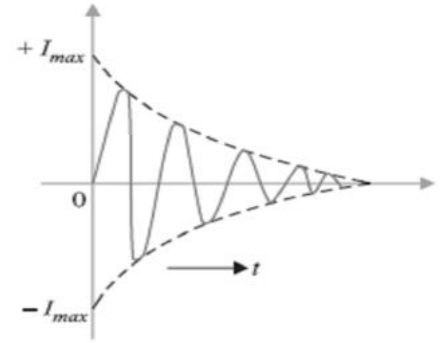
♣ **Frequency of oscillations.**

✎ The frequency of oscillations in the tank circuit is determined by the constants of the circuit viz L and C.

✎ The actual frequency of oscillations is the resonant frequency (or natural frequency) of the tank circuit given by :

$$f_r = \frac{1}{2\pi\sqrt{LC}}$$

✎ It is clear that frequency of oscillations in the tank circuit is inversely proportional to L and C. This can be easily explained.

✎ If a large value of capacitor is used, it will take longer for the capacitor to charge fully and also longer to discharge. This will lengthen the period of oscillations in the tank circuit, or equivalently lower its frequency.

✎ With a large value of inductance, the opposition to change in current flow is greater and hence the time required to complete each cycle will be longer.

✎ Therefore, the greater the value of inductance, the longer is the period or the lower is the frequency of oscillations in the tank circuit.

❖ **UNDAMPED OSCILLATIONS FROM TANK CIRCUIT:-**

✎ As discussed before, a tank circuit produces damped oscillations. However, in practice, we need continuous undamped oscillations for the successful operation of electronics equipment.

✎ In order to make the oscillations in the tank circuit undamped, it is necessary to supply correct amount of energy to the tank circuit at the proper time intervals to meet the losses.

✎ Thus referring back to Fig of tank circuit, any energy which would be applied to the circuit must have a polarity conforming to the existing polarity at the instant of application of energy.

✎ If the applied energy is of opposite polarity, it would oppose the energy in the tank circuit, causing stoppage of oscillations.

✎ Therefore, in order to make the oscillations in the tank circuit undamped, the following conditions must be fulfilled :

♣ **(i)** The amount of energy supplied should be such so as to meet the losses in the tank circuit and the a.c. energy removed from the circuit by the load.

✖ For instance, if losses in LC circuit amount to 5 mW and a.c. output being taken is 100 mW, then power of 105 mW should be continuously supplied to the circuit.

♣ **(ii)** The applied energy should have the same frequency as that of the oscillations in the tank circuit.

♣ **(iii)** The applied energy should be in phase with the oscillations set up in the tank circuit i.e. it should aid the tank circuit oscillations.

♣ If these conditions are fulfilled, the circuit will produce continuous undamped output as shown in Fig.
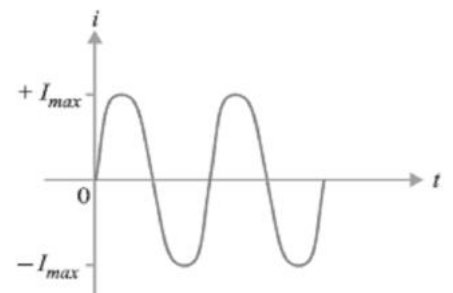
❖ **POSITIVE FEEDBACK AMPLIFIER — OSCILLATOR:-**

✍ A transistor amplifier with proper positive feedback can act as an oscillator i.e., it can generate oscillations without any external signal source.

✍ Fig shows a transistor amplifier with positive feedback. Remember that a positive feedback amplifier is one that produces a feedback voltage (V_f) that is in phase with the original input signal.

✍ As we can see, this condition is met in the circuit shown in Fig. A phase shift of 180° is produced by the amplifier and a further phase shift of 180° is introduced by feedback network.

✍ Thus, the signal is shifted by 360° and fed to the input i.e., feedback voltage is in phase with the input signal.

✍ **(i)** We note that the circuit shown in Fig is producing oscillations in the output. However, this circuit has an input signal. This is inconsistent with our definition of an oscillator i.e., an oscillator is a circuit that produces oscillations without any external signal source.

✍ **(ii)** When we open the switch S of Fig (i), we get the circuit shown in Fig (ii).This means the input signal (V_{in}) is removed. However, V_f (which is in phase with original signal) is still applied to the input signal.

✍ The amplifier will respond to this signal in the same way that it did to V_{in} i.e., V_f will be amplified and sent to the output. The feedback network sends a portion of the output back to the input.

✍ Therefore, the amplifier receives another input cycle and another output cycle is produced. This process will continue so long as the amplifier is turned on.

✍ Therefore, the amplifier will produce sinusoidal output with no external signal source. The following points may be noted carefully :

♣ A transistor amplifier with proper positive feedback will work as an oscillator.

♣ The circuit needs only a quick trigger signal to start the oscillations.

♣ Once the oscillations have started, no external signal source is needed.

♣ In order to get continuous undamped output from the circuit, the following condition must be met:

$$\boxed{m_v A_v = 1}$$

Where A_v = Voltage Gain of Amplifier without Feedback and m_v = Feedback Fraction

♣ This relation is called **Barkhausen Criterion**.

❖ **ESSENTIALS OF TRANSISTOR OSCILLATOR: -**

✍ Fig shows the block diagram of an oscillator. Its essential components are : -

♣ **Tank circuit**. It consists of inductance coil (L) connected in parallel with capacitor (C).

✍ The frequency of oscillations circuit depend upon the values of inductance of the coil and capacitance of the capacitor.

♣ **(ii) Transistor Amplifier.** The transistor amplifier receives D.C. power from the battery and changes it into a.c. power for supplying to the tank circuit.

✍ The oscillations occurring in the tank circuit are applied to the input of the transistor amplifier. Because of the amplifying properties of the transistor, we get increased output of these oscillations.

✍ This amplified output of oscillations is due to the D.C. power supplied by the battery.

✍ The output of the transistor can be supplied to the tank circuit to meet the losses.

♣ **(iii) Feedback Circuit**. The feedback circuit supplies a part of collector energy to the tank circuit in correct phase to aid the oscillations i.e. it provides positive feedback.
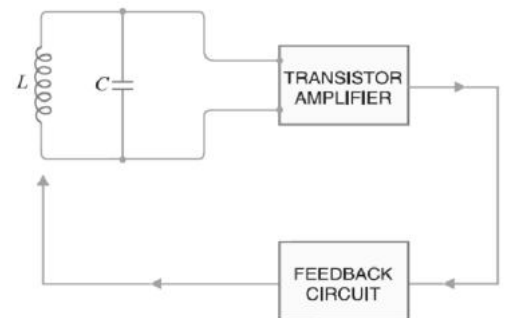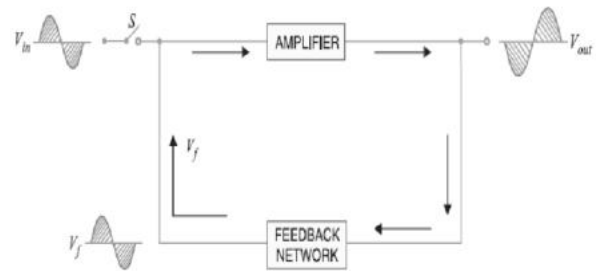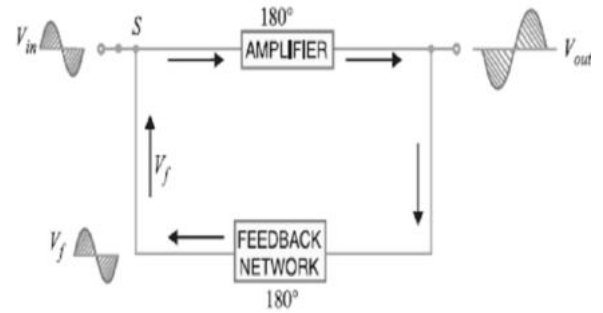
❖ EXPLANATION OF BARKHAUSEN CRITERION:-

✎ Barkhausen criterion is that in order to produce continuous undamped oscillations at the output of an amplifier, the positive feedback should be such that: $m_v A_v = 1$

✎ Once this condition is set in the positive feedback amplifier, continuous undamped oscillations can be obtained at the output immediately after connecting the necessary power supplies.

♣ **(i) Mathematical Explanation.** The voltage gain of a positive feedback amplifier is given by;

$$A_{vf} = \frac{A_V}{1 - A_V m_V} \qquad \rightarrow \quad \text{If } m_v A_v = 1, \quad \text{then } A_{vf} \rightarrow \infty.$$

✎ We know that we cannot achieve infinite gain in an amplifier. So what does this result infer in physical terms? It means that a vanishing small input voltage would give rise to finite (i.e., a definite amount of) output voltage even when the input signal is zero.

✎ Thus once the circuit receives the input trigger, it would become an oscillator, generating oscillations with no external signal source.

✎ **(ii) Graphical Explanation**. Let us discuss the condition $m_v A_v = 1$ graphically. Suppose the voltage gain of the amplifier without positive feedback is 100.

✎ In order to produce continuous undamped oscillations, $m_v A_v = 1$ or $m_v \times 100 = 1$ or $m_v = 0.01$.

✎ This is illustrated in Fig. Since the condition $m_v A_v = 1$ is met in the circuit shown in Fig, it will produce sustained oscillations.
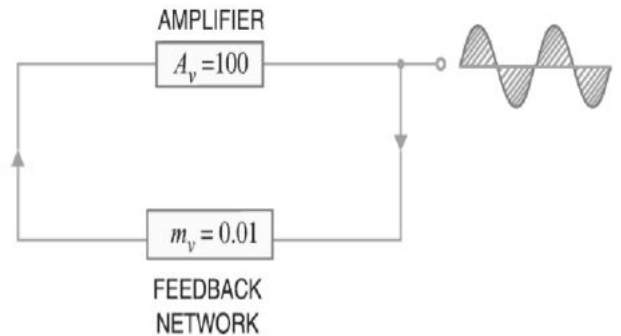
✎ Suppose the initial triggering voltage is 0.1V peak. Starting with this value, circuit ($A_v = 100$; $m_v = 0.01$) will progress as follows.

Cycle	V_{in}	V_{out}	V_f
1.	0.1Vpk	10Vpk	0.1Vpk
2.	0.1Vpk	10Vpk	0.1Vpk

✎ The same thing will repeat for 3rd, 4th cycles and so on. Note that during each cycle, $V_f = 0.1$Vpk and $V_{out} = 10$ Vpk. Clearly, the oscillator is producing continuous undamped oscillations.

✎ The relation $m_v A_v = 1$ holds good for true ideal circuits. However, practical circuits need an $m_v A_v$ product that is slightly greater than 1. This is to compensate for power loss (in resistors) in the circuit.

❖ DIFFERENT TYPES OF TRANSISTOR OSCILLATORS:-

✎ A transistor can work as an oscillator to produce continuous undamped oscillations of any desired frequency if tank and feedback circuits are properly connected to it.

✎ All oscillators under different names have similar function i.e., they produce continuous undamped output. However, the major difference between these oscillators lies in the method by which energy is supplied to the tank circuit to meet the losses.

✎ The following are the transistor oscillators commonly used at various places in electronic circuits:
 (i)   **Tuned Collector Oscillator** (ii) **Colpitt's Oscillator**
  (iii) **Hartley Oscillator**   (iv) **Phase Shift Oscillator**
  (v) **Wien Bridge Oscillator**   (vi) **Crystal Oscillator**

❖ TUNED COLLECTOR OSCILLATOR:-

✎ Fig shows circuit of tuned collector oscillator. It contains tuned circuit $L_1 - C_1$ in the collector and hence the name.

✎ The frequency of oscillations depends upon the values of L_1 and C_1 and is given by :

$$f = \frac{1}{2\pi\sqrt{L_1 C_1}}$$

✎ The feedback coil L_2 in the base circuit is magnetically coupled to the tank circuit coil L_1. In practice, L_1 and L_2 form the primary and secondary of the transformer respectively. The biasing is provided by potential divider arrangement. The capacitor C connected in the base circuit provides low reactance path to the oscillations.
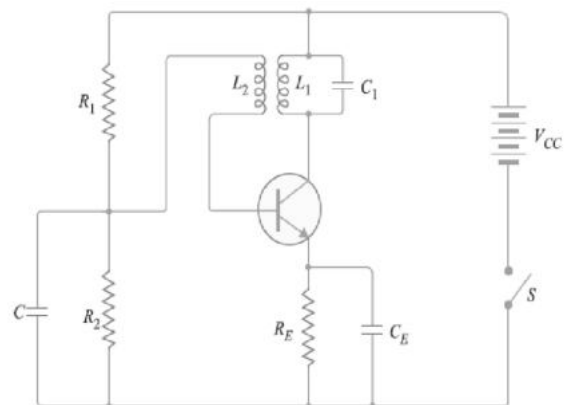
♣ **Circuit Operation**. When switch S is closed, collector current starts increasing and charges the capacitor C_1. When this capacitor is fully charged, it discharges through coil L_1, setting up oscillations of frequency determined by above equation.

✎ These oscillations induce some voltage in coil L_2 by mutual induction. The frequency of voltage in coil L_2 is the same as that of tank circuit but its magnitude depends upon the number of turns of L_2 and coupling between L_1 and L_2.

✎ The voltage across L_2 is applied between base and emitter and appears in the amplified form in the collector circuit, thus overcoming the losses occurring in the tank circuit.

✎ The number of turns of L_2 and coupling between L_1 and L_2 are so adjusted that oscillations across L_2 are amplified to a level just sufficient to supply losses to the tank circuit.

✎ It may be noted that the phase of feedback is correct i.e. energy supplied to the tank circuit is in phase with the generated oscillations. A phase shift of 180º is created between the voltages of L_1 and L_2 due to transformer action.

✎ A further phase shift of 180º takes place between base-emitter and collector circuit due to transistor properties. As a result, the energy feedback to the tank circuit is in phase with the generated oscillations.

❖ **COLPITT'S OSCILLATOR:-**

✎ Fig shows a Colpitt's oscillator. It uses two capacitors and placed across a common inductor L and the centre of the two capacitors is tapped.

✎ The tank circuit is made up of C_1, C_2 and L. The frequency of oscillations is determined by the values of C_1, C_2 and L and is given by ;

$$f = \frac{1}{2\pi\sqrt{LC_T}}$$

Where $\quad C_T = \frac{c_1 c_2}{c_1 + c_2}$
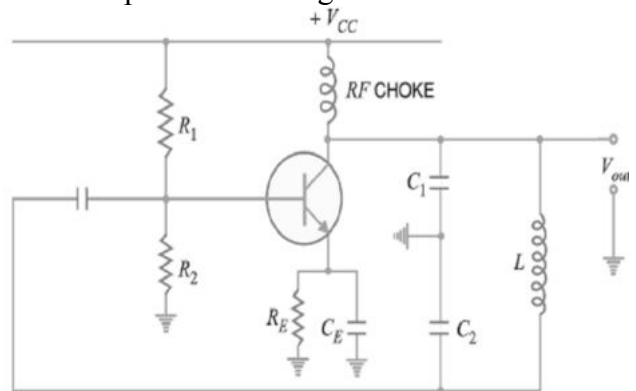
✡ Note that $C_1 - C_2 - L$ is also the feedback circuit that produces a phase shift of 180°.

♣ **Circuit Operation.** When the circuit is turned on, the capacitors C_1 and C_2 are charged. The capacitors discharge through L, setting up oscillations of frequency determined by exp.(i).

✎ Output voltage of the amplifier appears across C_1 and feedback voltage is developed across C_2. The voltage across it is 180° out of phase with the voltage developed across C_1 (V_{out}) as shown in Fig.

✎ It is easy to see that voltage feedback (voltage across C_2) to the transistor provides positive feedback.

✎ A phase shift of 180° is produced by transistor and a further phase shift of 180° is produced by $C_1 - C_2$ voltage divider.

✎ In this way, feedback is properly phased to produce continuous undamped oscillation.

✎ **Feedback fraction m_v.** The amount of feedback voltage in Colpitt's oscillator depends upon feedback fraction m_v of the circuit. For this circuit, Feedback fraction,

$$m_v = \frac{V_f}{V_{out}} = \frac{X_{c2}}{X_{c1}} = \frac{C_1}{C_2}$$

❖ **HARTLEY OSCILLATOR:-**

✎ The Hartley oscillator is similar to Colpitt's oscillator with minor modifications. Instead of using tapped capacitors, two inductors L_1 and L_2 are placed across a common capacitor C and the centre of the inductors is tapped as shown in Fig.

✎ The tank circuit is made up of L_1, L_2 and C. The frequency of oscillations is determined by the values of L_1, L_2 and C and is given by :

$$f = \frac{1}{2\pi\sqrt{CL_T}}$$ ……….. (i)

Where $\quad L_T = L_1 + L_2 + 2M$

Here M= mutual inductance between L_1 and L_2

✡ Note that $L_1 - L_2 - C$ is also the feedback network that produces a phase shift of 180°.
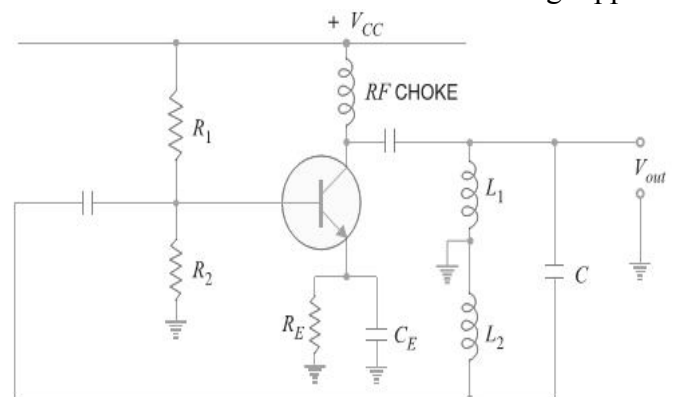
♣ **Circuit Operation**. When the circuit is turned on, the capacitor is charged. When this capacitor is fully charged, it discharges through coils L_1 and L_2 setting up oscillations of frequency determined by equ (i).

✍ The output voltage of the amplifier appears across L_1 and feedback voltage across L_2. The voltage across L_2 is 180° out of phase with the voltage developed across L_1 (V_{out}) as shown in Fig.

✍ It is easy to see that voltage feedback (i.e., voltage across L_2) to the transistor provides positive feedback.

✍ A phase shift of 180° is produced by the transistor and a further phase shift of 180° is produced by $L_1 - L_2$ voltage divider.

✍ In this way, feedback is properly phased to produce continuous undamped oscillations.

✍ **Feedback fraction m_v.** In Hartley oscillator, the feedback voltage is across L_2 and output voltage is across L_1.
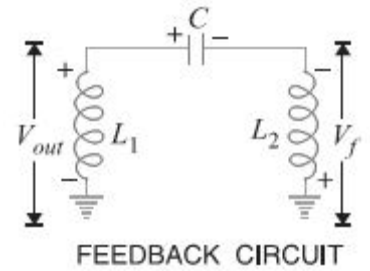
$$m_v = \frac{V_f}{V_{out}} = \frac{X_{L2}}{X_{L1}} = \frac{L_1}{L_2}$$

❖ **PRINCIPLE OF PHASE SHIFT OSCILLATORS:-**

✍ One desirable feature of an oscillator is that it should feedback energy of correct phase to the tank circuit to overcome the losses occurring in it.

✍ In the oscillator circuits discussed so far, the tank circuit employed inductive (L) and capacitive (C) elements. In such circuits, a phase shift of 180º was obtained due to inductive or capacitive coupling and a further phase shift of 180º was obtained due to transistor properties.

✍ In this way, energy supplied to the tank circuit was in phase with the generated oscillations. The oscillator circuits employing L-C elements have two general drawbacks.

✍ **Firstly**, they suffer from frequency instability and poor waveform. **Secondly**, they cannot be used for very low frequencies because they become too much bulky and expensive.

✍ Good frequency stability and waveform can be obtained from oscillators employing resistive and capacitive elements. Such amplifiers are called R-C or phase shift oscillators and have the additional advantage that they can be used for very low frequencies.

✍ In a phase shift oscillator, a phase shift of 180º is obtained with a phase shift circuit instead of inductive or capacitive coupling.

✍ A further phase shift of 180º is introduced due to the transistor properties. Thus, energy supplied back to the tank circuit is assured of correct phase.

✍ **Phase shift Circuit.** A phase-shift circuit essentially consists of an R-C network. Fig (i) shows a single section of RC network. From the elementary theory of electrical engineering, it can be shown that alternating voltage V'_1 across R leads the applied voltage V_1 by φº. The value of φ depends upon the values of R and C.

✍ If resistance R is varied, the value of φ also changes. If R were reduced to zero, V'_1 will lead V_1 by 90º i.e. φ = 90º.

✍ However, adjusting R to zero would be impracticable because it would lead to no voltage across R.
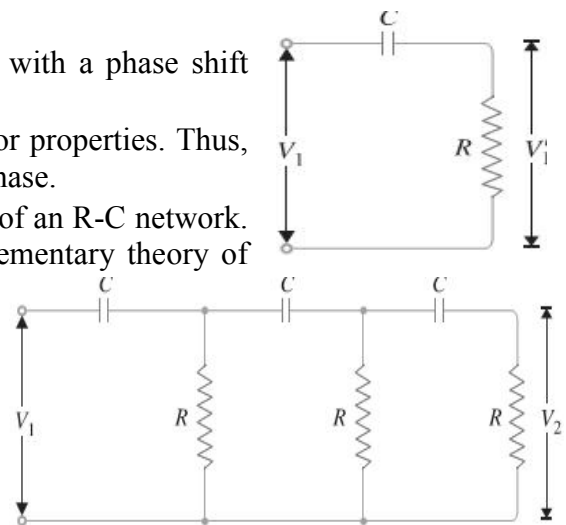
✍ Therefore, in practice, R is varied to such a value that makes V'_1 to lead V_1 by 60º.

✍ Fig (ii) shows the three sections of RC network. Each section produces a phase shift of 60º. Consequently, a total phase shift of 180º is produced i.e. voltage V_2 leads the voltage V_1 by 180º.

❖ **PHASE SHIFT OSCILLATOR:-**

✍ Fig. shows the circuit of a phase shift oscillator. It consists of a conventional single transistor amplifier and a RC phase shift network.

✍ The phase shift network consists of three sections R_1C_1, R_2C_2 and R_3C_3. At some particular frequency f_0, the phase shift in each RC section is 60º so that the total phase-shift produced by the RC network is 180º.

✍ The frequency of oscillations is given by:

$$f_0 = \frac{1}{2\pi\,RC\sqrt{6}}$$

Where $R_1 = R_2 = R_3 = $ **R**   & $C_1 = C_2 = C_3 = $ **C**

♣ **Circuit Operation.** When the circuit is switched on, it produces oscillations of frequency determined by exp. (i). The output E_0 of the amplifier is fed back to RC feedback network.

🐦 This network produces a phase shift of 180º and a voltage Ei appears at its output which is applied to the transistor amplifier.

🐦 Obviously, the feedback fraction m= E_i/E_0. The feedback phase is correct. A phase shift of 180º is produced by the transistor amplifier.

🐦 A further phase shift of 180º is produced by the RC network. As a result, the phase shift around the entire loop is 360º.

♣ **Advantages**
  ✖ It does not require transformers or inductors.
  ✖ It can be used to produce very low frequencies.
  ✖ The circuit provides good frequency stability.

♣ **Disadvantages**
  ✖ It is difficult for the circuit to start oscillations as the feedback is generally small.
 ✖ The circuit gives small output.
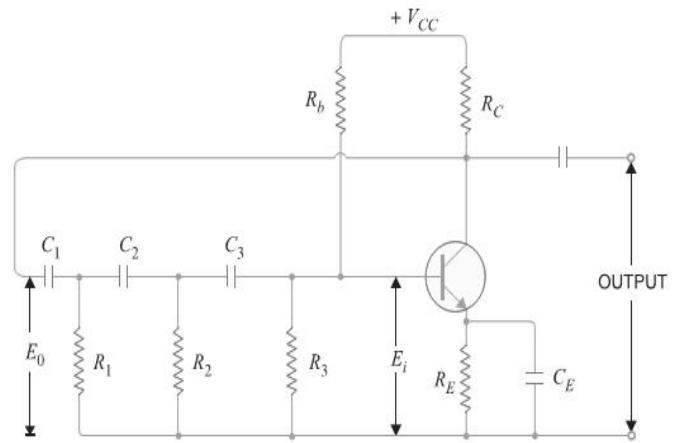
❖ **WIEN BRIDGE OSCILLATOR:-**

🐦 The Wien-bridge oscillator is the standard oscillator circuit for all frequencies in the range of 10 Hz to about 1 MHz. It is the most frequently used type of audio oscillator as the output is free from circuit fluctuations and ambient temperature.

🐦 Fig. shows the circuit of Wien bridge oscillator. It is essentially a two-stage amplifier with R-C bridge circuit. The bridge circuit has the arms R_1C_1, R_3, R_2C_2 and tungsten lamp L_p.

🐦 Resistances R_3 and L_p are used to stabilize the amplitude of the output. The transistor T_1 serves as an oscillator and amplifier while the other transistor T_2 serves as an inverter (to produce 180º phase shift).

🐦 The circuit uses positive and negative feedbacks. The positive feedback is through R_1C_1, C_2R_2 to the transistor T_1. The negative feedback is through the voltage divider to the input of transistor T_2.

🐦 The frequency of oscillations is determined by the series element R_1C_1 and parallel element R_2C_2 of the bridge.

$$f = \frac{1}{2\pi\sqrt{R_1 \, C_1 \, R_2 C_2}}$$ If $R_1 = R_2 = R$ and $C_1 = C_2 = C$, then, $$f = \frac{1}{2\pi RC}$$

🐦 When the circuit is started, bridge circuit produces oscillations of frequency determined.

🐦 The two transistors produce a total phase shift of 360º so that proper positive feedback is ensured.

🐦 The negative feedback in the circuit ensures constant output. This is achieved by the temperature sensitive tungsten lamp L_p. Its resistance increases with current.

🐦 Should the amplitude of output tend to increase, more current would provide more negative feedback.

🐦 The result is that the output would return to original value.

🐦 A reverse action would take place if the output tends to decrease.
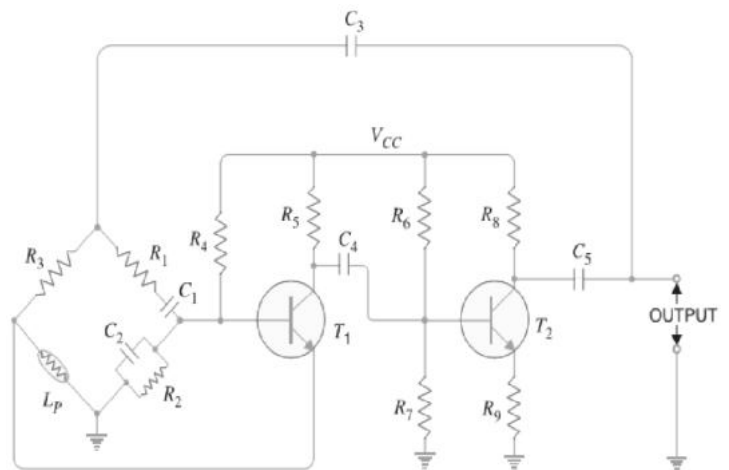
♣ **Advantages**
  (i) It gives constant output. **(ii)** It works quite easily. **(iii)** Overall gain is high due to two transistors.
  (iv) The frequency of oscillations can be easily changed by using a potentiometer.

♣ **Disadvantages**
 (i) It requires two transistors & large number of components. **(ii)** It cannot generate very high frequencies.

❖ **LIMITATIONS OF LC AND RC OSCILLATORS:-**

✎ The LC and RC oscillators discussed so far have their own limitations. The major problem in such circuits is that their operating frequency does not remain strictly constant. There are two principal reasons for it viz.,

♣ (i) As the circuit operates, it will warm up. Consequently, the values of resistors and inductors, which are the frequency determining factors in these circuits, will change with temperature.

♣ This causes the change in frequency of the oscillator.

♣ (ii) If any component in the feedback network is changed, it will shift the operating frequency of the oscillator.

✎ However, in many applications, it is desirable and necessary to maintain the frequency constant with extreme low tolerances.

✎ It is apparent that if we employ LC or RC circuits, a change of temperature may cause the frequencies of adjacent broadcasting stations to overlap.

✎ In order to maintain constant frequency, piezoelectric crystals are used in place of LC or RC circuits. Oscillators of this type are called crystal oscillators.

✎ The frequency of a crystal oscillator changes by less than 0.1% due to temperature and other changes.

✎ Therefore, such oscillators offer the most satisfactory method of stabilizing the frequency and are used in great majority of electronic applications.

❖ **PIEZOELECTRIC CRYSTALS:-**

✎ Certain crystalline materials, namely, *Rochelle salt, quartz and tourmaline* exhibit the **piezoelectric effect** i.e., when we apply an a.c. voltage across them, they vibrate at the frequency of the applied voltage. Conversely, when they are compressed or placed under mechanical strain to vibrate, they produce an a.c. voltage.

✎ Such crystals which exhibit piezoelectric effect are called **piezoelectric crystals**. Of the various piezoelectric crystals, **quartz** is most commonly used as it is inexpensive and readily available in nature.

✎ **Quartz Crystal**. Quartz crystals are generally used in crystal oscillators because of their great mechanical strength and simplicity of manufacture.

✎ The natural shape of quartz crystal is hexagonal as shown in Fig. The three axes are shown: the z-axis is called the optical axis, the x-axis is called the electrical axis and y-axis is called the mechanical axis.

✎ Quartz crystal can be cut in different ways. Crystal cut perpendicular to the x-axis is called **x-cut crystal** whereas that cut perpendicular to y-axis is called **y-cut crystal**. The piezoelectric properties of a crystal depend upon its cut.

✎ **Frequency of Crystal.** Each crystal has a natural frequency like a pendulum. The natural frequency f of a crystal is given by: $\mathbf{f} = \frac{K}{t}$ Where,

    K = Constant that depends upon the cut **&** **t** = Thickness of the crystal.

✎ It is clear that frequency is inversely proportional to crystal thickness. The thinner the crystal, the greater is its natural frequency and vice-versa.

✎ However, extremely thin crystal may break because of vibrations. This puts a limit to the frequency obtainable. In practice, frequencies between 25 kHz to 5 MHz have been obtained with crystals.

❖ **WORKING OF QUARTZ CRYSTAL:-**

✎ In order to use crystal in an electronic circuit, it is placed between two metal plates. The arrangement then forms a capacitor with crystal as the dielectric as shown in Fig.

✎ If an a.c. voltage is applied across the plates, the crystal will start vibrating at the frequency of applied voltage. However, if the frequency of the applied voltage is made equal to the natural frequency of the crystal, resonance takes place and crystal vibrations reach a maximum value.

✎ This natural frequency is almost constant. Effects of temperature change can be eliminated by mounting the crystal in a temperature-controlled oven as in radio and television transmitters.
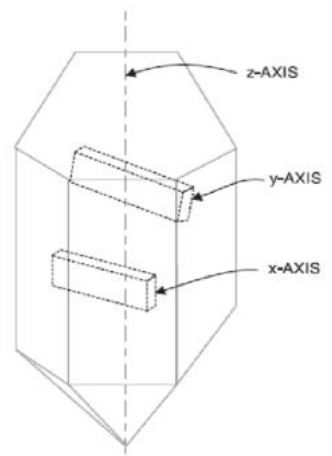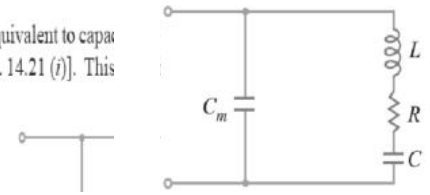
❖ **Equivalent Circuit of Crystal:-**

✎ Although the crystal has electromechanical resonance, we can represent the crystal action by an equivalent electrical circuit.

✎ (i) When the crystal is not vibrating, it is equivalent to capacitance C_m because it has two metal plates separated by a dielectric [See Fig (i)].

, it is equivalent to capac See Fig. 14.21 (i)]. This

✎ This capacitance is known as **mounting capacitance**.

✎ (ii) When a crystal vibrates, it is equivalent to R–L– C series circuit. Therefore, the equivalent circuit of a vibrating crystal is R– L– C series circuit shunted by the mounting capacitance C_m as shown in Fig (ii).

C_m = mounting capacitance **&** R–L–C = electrical equivalent of vibrational characteristic of the crystal

❖ **TRANSISTOR CRYSTAL OSCILLATOR:-**

✎ Fig. shows the transistor crystal oscillator. Note that it is a Collpit's oscillator modified to act as a crystal oscillator.

✎ The only change is the addition of the crystal (Y) in the feedback network. The crystal will act as a parallel-tuned circuit.

✎ As we can see in this circuit that instead of Fig. resonance caused by L and $(C_1 + C_2)$, we have the parallel resonance of the crystal. At parallel resonance, the impedance of the crystal is maximum.
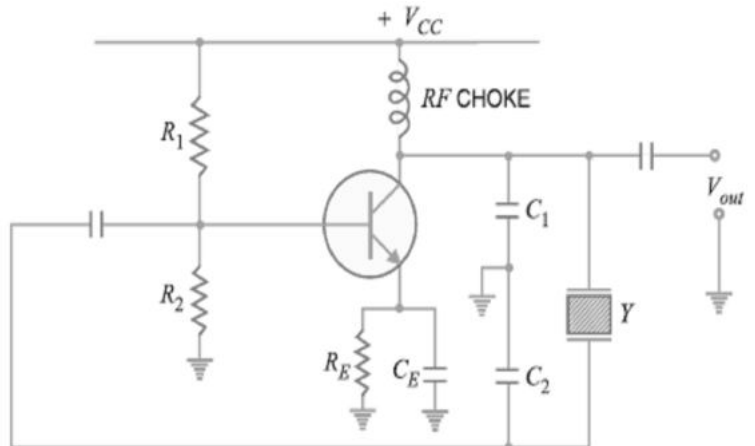
✎ This means that there is a maximum voltage drop across C_1. This in turn will allow the maximum energy transfer through the feedback network at f_p.

✎ Note that feedback is positive. A phase shift of 180° is produced by the transistor. A further phase shift of 180° is produced by the capacitor voltage divider.

✎ This oscillator will oscillate only at f_p. Even the smallest deviation from f_p will cause the oscillator to act as an effective short. Consequently, we have an extremely stable oscillator.

$$Q\text{-factor of crystal} \quad = \quad \frac{1}{R}\sqrt{\frac{L}{C}}$$

♣ **Advantages**
   ✖ They have a high order of frequency stability.
   ✖ The quality factor (Q) of the crystal is very high.

♣ **Disadvantages**
   ✖ They are fragile and consequently can only be used in low power circuits.
   ✖ The frequency of oscillations cannot be changed appreciably.

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[CHAPTER-7]

-------------------------------- [TUNED AMPLIFIER] --------------------------------

❖ **INTRODUCTION**

✎ Most of the audio amplifiers we have discussed in the earlier chapters will also work at radio frequencies *i.e.* above 50 kHz.

✎ However, they suffer from two major drawbacks. **First,** they become less efficient at radio frequency. **Secondly,** such amplifiers have mostly resistive loads and consequently their gain is independent of signal frequency over a large bandwidth.

✎ In other words, an audio amplifier amplifies a wide band of frequencies equally well and does not permit the selection of a particular desired frequency while rejecting all other frequencies.

✎ However, sometimes it is desired that an amplifier should be selective *i.e.* it should select a desired frequency or narrow band of frequencies for amplification.

✎ For instance, radio and television transmission are carried on a specific radio frequency assigned to the broadcasting station. The radio receiver is required to pick up and amplify the radio frequency desired while discriminating all others.

✎ To achieve this, the simple resistive load is replaced by a parallel tuned circuit whose impedance strongly depends upon frequency.

✎ Such a tuned circuit becomes very selective and amplifies very strongly signals of resonant frequency and narrow band on either side.

✎ Thus, the use of tuned circuits in conjunction with a transistor makes possible the selection and efficient amplification of a particular desired radio frequency. Such an amplifier is called a *tuned amplifier*.

✎ In this chapter, we shall focus our attention on transistor tuned amplifiers and their increasing applications in high frequency electronic circuits.

❖ **TUNED AMPLIFIERS**

✎ *Amplifiers which amplify a specific frequency or narrow band of frequencies are called **tuned amplifiers.***

✎ Tuned amplifiers are mostly used for the amplification of high or radio frequencies.

✎ It is because radio frequencies are generally single and the tuned circuit permits their selection and efficient amplification.

✎ Tuned amplifiers are widely used in radio and television circuits where they are called upon to handle radio frequencies.

✎ Fig. shows circuit of a simple transistor tuned amplifier. Here, instead of load resistor, a parallel tuned circuit in the collector.

✎ The impedance of this tuned circuit strongly depends upon frequency. It offers a very high impedance at *resonant frequency* and very small impedance at all other frequencies.

✎ If the signal has the same frequency as the resonant frequency of *LC* circuit, large amplification will result due to high impedance of *LC* circuit at this frequency.

✎ When signals of many frequencies are present at the input of tuned amplifier, it will select and strongly amplify the signals of resonant frequency while rejecting all others.

✎ Therefore, such amplifiers are very useful in radio receivers to select the signal from one particular broadcasting station when signals of many other frequencies are present at the receiving aerial.
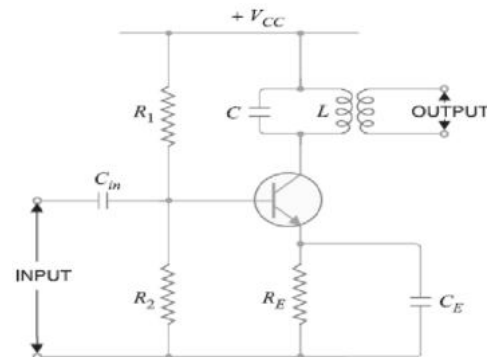
❖ **DIFFERENCE BETWEEN TUNED AMPLIFIERS AND OTHER AMPLIFIERS : -**

✎ We have seen that amplifiers (*e.g.*, voltage amplifier, power amplifier *etc.*) provide the constant gain over a limited band of frequencies *i.e.*, from lower cut-off frequency f_1 to upper cut-off frequency f_2. Now bandwidth of the amplifier, $BW = f_2 - f_1$.

✎ The difference is that tuned amplifiers are designed to have specific, usually narrow bandwidth. This is explained in the Fig.

✎ Note that BW_S is the bandwidth of standard frequency response while BW_T is the bandwidth of the tuned amplifier.

✎ In many applications, the narrower the bandwidth of a tuned amplifier, the better it is.
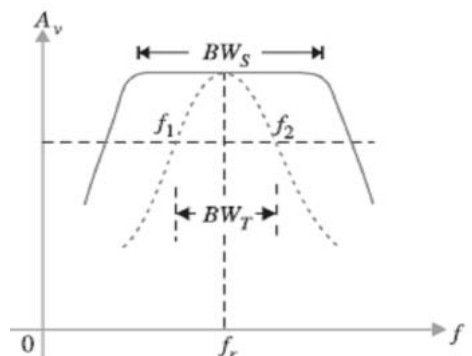
❖ ANALYSIS OF PARALLEL TUNED CIRCUIT : -

- ✎ A parallel tuned circuit consists of a capacitor *C* and inductor *L* connected in parallel to each other with respect to a supply source.
- ✎ Fig. shows a parallel resonant circuit connected across an ac supply source of variable frequency.
- ✎ Here the resistance R represents the coil resistance. Its value is usually very small and the order of few ohms and hence it can be neglected as compare to the impedance of the resonance circuits.
- ✎ Now consider the frequency of the ac supply to be varied suitably. As a result of this, the circuit will encounter different impedance at different frequencies.
- ✎ As the frequency is increased the inductive reactance $[X_L]$ is also increased and the capacitive reactance $[X_C]$ is increased. There is a certain frequency of the applied ac voltage at which the inductive reactance is equal to the capacitive reactance. This frequency is called **resonance frequency.** It is designated by f_0.
- ✎ The frequency at which parallel resonance occurs (*i.e.* reactive component of circuit current becomes zero) is called the ***resonant frequency*** f_0.
- ✎ At resonant frequency, the circuit is said to be in electrical resonance. Under resonance condition the impendence of the resonant circuits becomes maximum and the line current (i.e. the current drawn from the source) is minimum.
- ✎ The expression for resonance frequency may be obtained from the condition,

$$X_L = X_C \qquad \rightarrow \qquad 2\pi f_0 L = \frac{1}{2\pi f_0 C} \qquad \rightarrow \qquad f_0^2 = \frac{1}{4\pi^2 LC} \qquad \rightarrow \qquad \boxed{f_0 = \frac{1}{2\pi\sqrt{LC}}}$$

- ✎ If value of inductance is Henry & the capacitance is farads Hertz then the resonance frequency is Hertz.

❖ RESONANCE CURVE : -

- ✎ It is a curve, which shows the variation of **circuit impedance** (or circuit current) with the change in **frequency** of the applied voltage.
- ✎ Fig. shows the variation of circuit impedance (Z_p) with change in frequency of the applied voltage.
- ✎ From the fig it is clear that the impedance is maximum at the resonance and is equal to L/CR. If the frequency is changed above or below the resonance, the value of impedance decreases rapidly.
- ✎ If f_1 and f_2 are the lower & higher cutoff frequencies then Band width **BW=f_2-f_1**.

❖ SHARPNESS OF RESONANCE: -

- ✎ The resonance curve of a resonant circuit is required to be as sharp as possible in order to provide a high selectivity.
- ✎ The sharp resonance curve means that the impedance falls off rapidly as the frequency is varied above and below the resonant frequency.
- ✎ Mathematically the sharpness of a resonance curve is defined as ratio of the bandwidth of the circuit to its resonant frequency. i.e.

Sharpness of Resonance = Band Width / Resonant frequency
$$= BW/f_0 = f_2\text{-}f_1 / f_0 = 1 / Q_0$$

- ✎ Where Q_0 is called the quality factor or Q-Factor.
- ✎ The ratio of inductive reactance and resistance of the coil at resonance, therefore, becomes a measure of the quality of the tuned circuit.
- ✎ This is called quality factor and may be defined as under : The ratio of *inductive reactance of the coil at resonance to its resistance is known as* **quality factor Q** *i.e.* **Q = X_L/R= 2πfL/R**
- ✎ The quality factor *Q* of a parallel tuned circuit is very important as the sharpness of resonance curve and hence selectivity of the circuit depends upon it. Higher value of *Q*, more the selective of the tuned circuit.
- ✎ The smaller the resistance of coil, the sharper is the resonance curve. This is due to the fact that a small resistance consumes less power and draws a relatively small line current.
- ✎ Fig. shows the effect of resistance *R* of the coil on the sharpness of the resonance curve. It is clear that when resistance is small, the resonance curve is very sharp. However, if the coil has large resistance, the resonance curve is less sharp. So where high selectivity is desired, the value of *Q* should be very large.
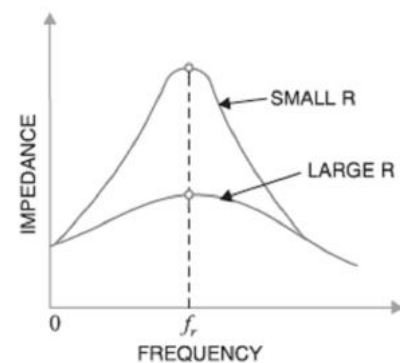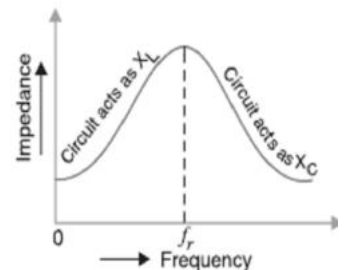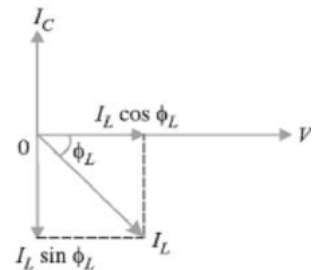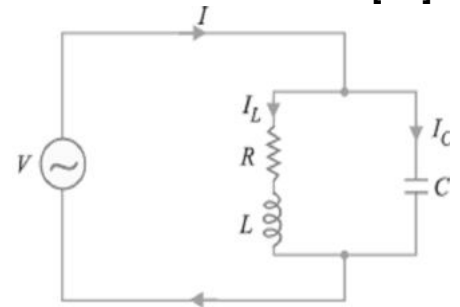
❖ **ADVANTAGES OF TUNED AMPLIFIERS: -**

✎ In high frequency applications, it is generally required to amplify a single frequency, rejecting all other frequencies present. For such purposes, tuned amplifiers are used. These amplifiers use tuned parallel circuit as the collector load and offer the following advantages :

    (***i***) **Small power loss.** (***ii***) **High selectivity.** (***iii***) **Smaller collector supply voltage.**

❖ **SINGLE TUNED AMPLIFIER : -**

✎ A single tuned amplifier consists of a transistor amplifier containing a parallel tuned circuit as the collector load. The values of capacitance and inductance of the tuned circuit are so selected that its resonant frequency is equal to the frequency to be amplified.

✎ The output from a single tuned amplifier can be obtained either (***a***) by a coupling capacitor C_C as shown in Fig (i) or (***b***) by a secondary coil as shown in Fig (***ii***).

✎ Fig (i) is also called as single tuned voltage amplifier using Capacitive Coupled where as fig (ii) is called as single tuned voltage amplifier using Inductive Coupled.

✎ Both these circuits consist of a transistor amplifier and a tunes circuit as the load. The values of capacitance (C) and Inductance (L) of the tunes circuits are selected in such a way that the resonant frequency of the tunes circuit is equal to the frequency to be selected and amplified.

✎ The resistors R_1, R_2 and R_E are called biasing resisters. These resistors provide the d.c. operating current and voltage for the transistor.


    (i)   (ii)
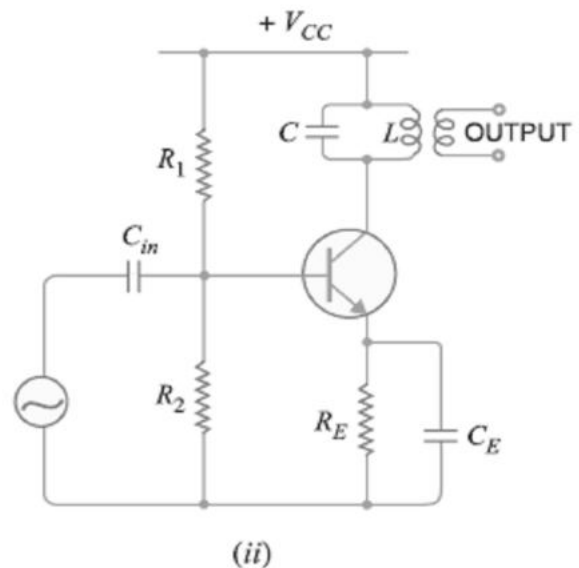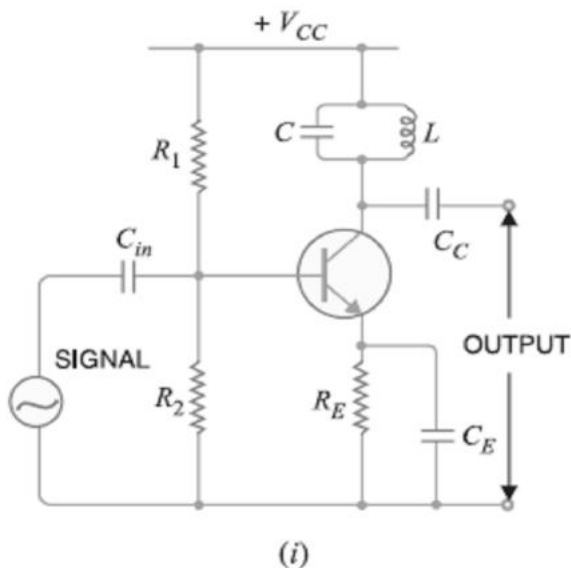
❖ **OPERATION.**

✎ The high frequency signal i.e. radio frequency signal to be amplified is given to the input of the amplifier.

✎ The resonant frequency of parallel tuned circuit is made equal to the frequency of the signal by changing the value of C.

✎ Under such conditions, the tuned circuit will offer very high impedance to the signal frequency. Hence a large output appears across the tuned circuit.

✎ In case the input signal is complex containing many frequencies, only that frequency which corresponds to the resonant frequency of the tuned circuit will be amplified.

✎ All other frequencies will be rejected by the tuned circuit. In this way, a tuned amplifier selects and amplifies the desired frequency.

❖ **Frequency Response of Single Tuned Voltage Amplifiers : -**

✎ At the resonant frequency, the impedance of the parallel resonant circuit is very high and is purely resistive.

✎ Therefore, when the circuit is tuned to resonant frequency, the voltage across R_L is maximum.

❖ In other words, the voltage gain is maximum at f_r. However, above and below the resonant frequency, the voltage gain decreases rapidly.

❖ The higher the Q of the circuit, the faster the gain drops off on either side of resonance.
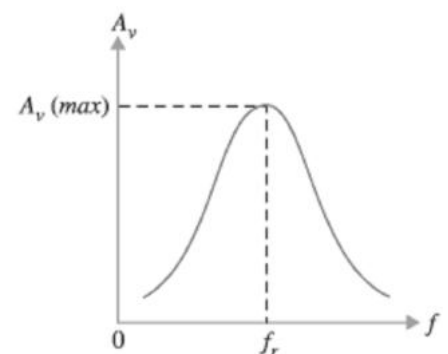
❖ LIMITATIONS OF SINGLE TUNED AMPLIFIER: -

- ➤ The tuned voltage amplifier, in communication receiver, is used to select the desired carrier frequency and amplifying the complete band of frequencies around the selected carrier frequency.
- ➤ In other word, tuned amplifiers are required to be high selectivity. But the high selectivity requires a tuned circuit with a high Q-factor.
- ➤ We also know that a high-Q circuit will give a high voltage gain. But, at the same time, it will give reduces bandwidth (Because band width is reciprocal to the Q-factor).
- ➤ It means that a tuned a tuned voltage amplifier with reduced band width may not be able to amplify equally the complete band of the transmitted signal.
- ➤ In other words, narrow band width or smaller pass band of the amplifier will result in a poor reproduction of the audio signal.
- ➤ It is the major limitation of a single tuned voltage amplifier & is overcome by using double tuned circuit.

❖ <u>DOUBLE TUNED AMPLIFIER</u> : -

- ➤ Fig shows the circuit of a double tuned amplifier.
- ➤ It consists of a transistor amplifier containing two tuned circuits; one (L_1C_1) in the collector and the other (L_2C_2) in the output as shown.
- ➤ The resistors R_1, R_2 and R_E are used to provide d.c. current and voltage for transistor operation.
- ➤ The high frequency signal to be amplified is applied to the input terminals of the amplifier.
- ➤ The resonant frequency of tuned circuit L_1C_1 is made equal to the signal frequency.
- ➤ Under such conditions, the tuned circuit offers very high impedance to the signal frequency.
- ➤ Hence, large output appears across the tuned circuit L_1C_1.
- ➤ The output from this tuned circuit is transferred to the second tuned circuit L_2C_2 through mutual induction. Double tuned circuits are extensively used for coupling the various circuits of radio and television receivers.
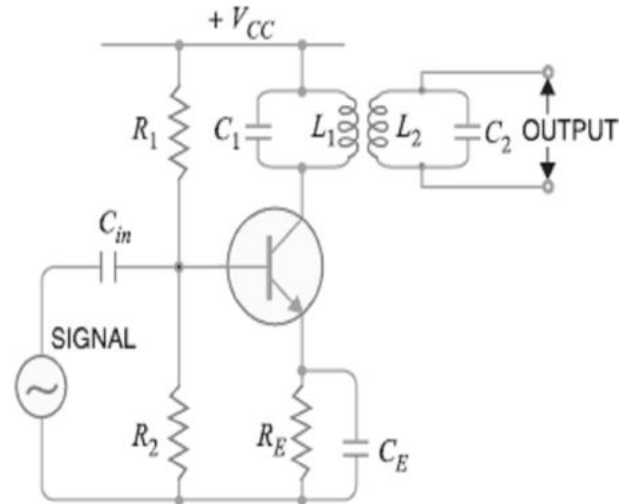
❖ FREQUENCY RESPONSE OF DOUBLE TUNED VOLTAGE AMPLIFIERS : -
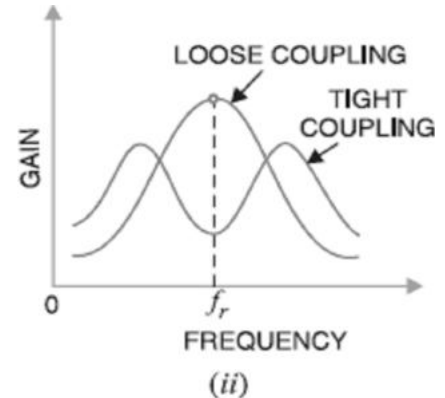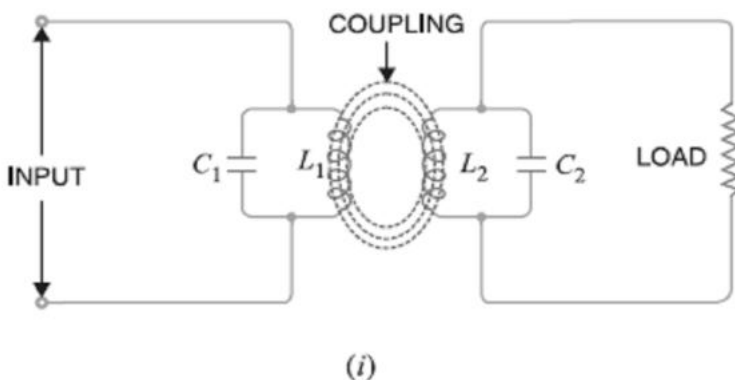
- ➤ The frequency response of a double tuned circuit depends upon the degree of coupling *i.e.* upon the amount of mutual inductance between the two tuned circuits.
- ➤ When coil L_2 is coupled to coil L_1 [See Fig. (*i*)], a portion of load resistance is coupled into the primary tank circuit L_1C_1 and affects the primary circuit in exactly the same manner as though a resistor had been added in series with the primary coil L_1.
- ➤ When the coils are spaced apart, all the primary coil L_1 flux will not link the secondary coil L_2. The coils are said to have *loose coupling*.
- ➤ Under such conditions, the resistance reflected from the load (*i.e.* secondary circuit) is small. The resonance curve will be sharp and the circuit Q is high as shown in Fig. (*ii*).
- ➤ When the primary and secondary coils are very close together, they are said to have ***tight coupling***. Under such conditions, the reflected resistance will be large and the circuit Q is lower.
- ➤ Two positions of gain maxima, one above and the other below the resonant frequency, are obtained.

❖ **BANDWIDTH OF DOUBLE–TUNED CIRCUIT: -**

✎ If you refer to the frequency response of double-tuned circuit shown in Fig. (*ii*), it is clear that bandwidth increases with the degree of coupling.

✎ Obviously, the determining factor in a double tuned circuit is not Q but the coupling. For a given frequency, the tighter the coupling, the greater is the bandwidth. **$BW_{dt} = k\ f_r$**

✎ The subscript *dt* is used to indicate double-tuned circuit. Here *k* is coefficient of coupling.

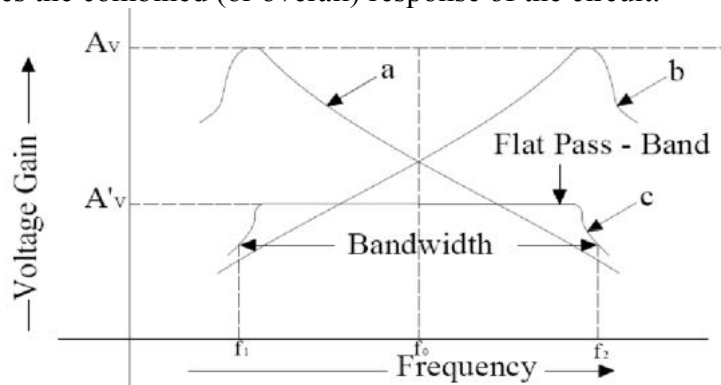✡ It Provides **High Selectivity**, **High Gain** and relatively **Large Band Width** to tuned circuit.

❖ **STAGGER-TUNED VOLTAGE AMPLIFIER : -**

✎ It has been observed that if two or more tuned circuits, which are synchronously tuned are cascaded, the overall bandwidth decreases.

✎ However, if the different tuned circuits which are cascaded, are tuned to slightly different frequencies, it is possible to obtain an increased bandwidth with a flat pass band with steep sides.

✎ This technique is known as **Stagger-Tuning**.
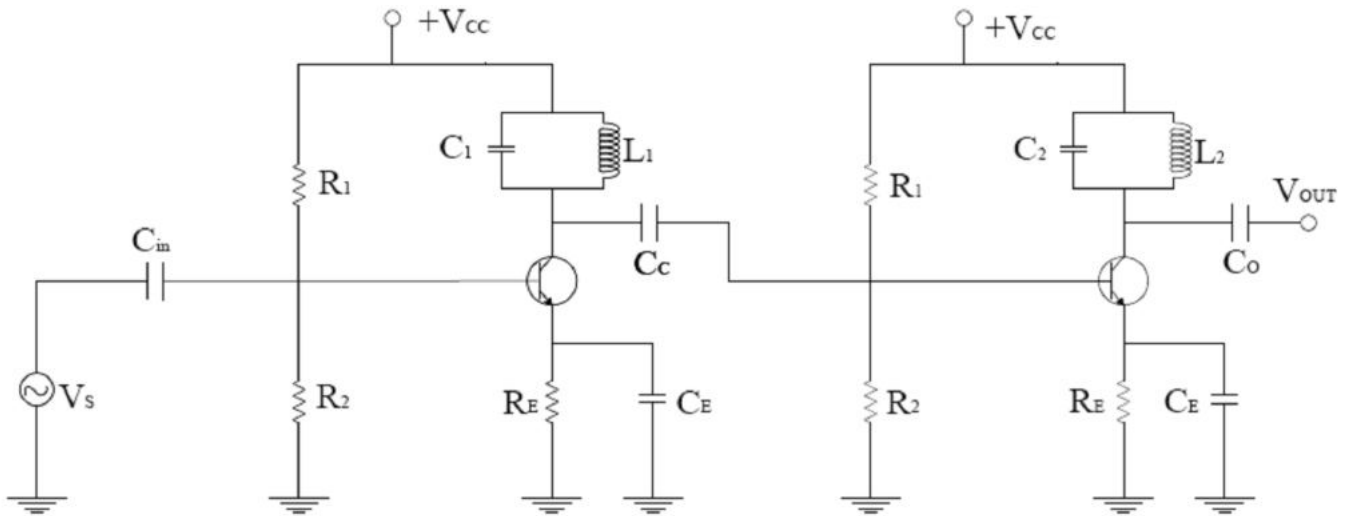
[Two-Stage Stagger Tuned Voltage Amplifier]

✎ The above Fig shows a two stage tuned voltage amplifier. The stagger tuning in this circuit, may be achieved by resonating the tuned circuit L_1C_1 and L_2C_2 to slightly different frequencies.

✎ The figure below shows the frequency response of a stagger-tuned amplifier. In this figure, curve **'a'** shows the gain verses frequency response of the L_1C_1 tuned circuit.

✎ Similarly the curve 'b' shows the gain verses frequency response of the L2C2 tuned circuit.

✎ The curve **'c'** indicates the combined (or overall) response of the circuit.

[Frequency Responce of a Stagger - Tuned Voltage Amplifier]

✎ It is clear from this circuit that the amplifier has a greater bandwidth and flatter pass-band. It has been found that more the pass band and stepper will be the gain fall-off outside the pass band.

✎ It is noted that because of stagger-tuning, there is a loss of voltage gain (Gain reduces from A_v to $A^`_v$).

✎ If an optimum stager-tuning is employed, the response curve of the amplifier is very close to a rectangular response curve. Such a response is known as **Butterworth Response.**

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[CHAPTER-8]

[COMMON APPLICATION OF DIODE, TRANSISTOR & WAVE SHAPING CIRCUIT]

❖ **INTRODUCTION**

✎ We have seen that diodes can be used as rectifiers. Apart from this, diodes have many other applications.

✎ However, we shall confine ourselves to the following two applications of diodes :-

   **(i)** As a **Clipper**   **(ii)** As a **Clamper**

✎ A **clipper** (or limiter) is used to clip off or remove a portion of an a.c. signal. The half-wave rectifier is basically a clipper that eliminates one of the alternations of an a.c. signal.

✎ A **clamper** (or dc restorer) is used to restore or change the dc reference of an ac signal. For example, you may have a 10 V pp ac signal that varies equally above and below 2 V dc.

❖ **CLIPPING CIRCUITS :-**

✎ The circuit with which the waveform is shaped by removing (or clipping) a portion of the applied wave is known as a **clipping circuit.**

✎ Clippers find extensive use in radar, digital and other electronic systems. Although several clipping circuits have been developed to change the wave shape, we shall confine our attention to diode clippers.

✎ These clippers can remove signal voltages above or below a specified level.

✎ The important diode clippers are **(i) Positive** Clipper **(ii) Biased** Clipper **(iii) Combination** Clipper.

♣ **POSITIVE CLIPPER: -**

✎ A positive clipper is that which removes the positive half-cycles of the input voltage. Fig. shows the typical circuit of a positive clipper using a diode.
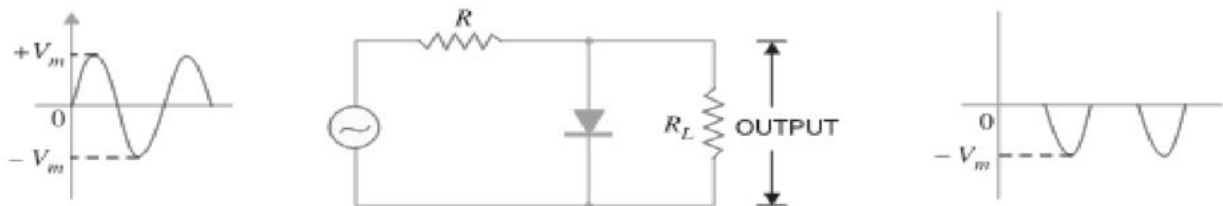
✎ As shown, the output voltage has all the positive half-cycles removed or clipped off.

✎ The circuit action is as follows**: -** During the positive half-cycle of the input voltage, the diode is forward biased and conducts heavily.

✎ Therefore, the voltage across the diode (which behaves as a short) and hence the output voltage across the load R is zero. Hence output voltage during positive half-cycles is zero.

✎ During the negative half-cycle of the input voltage, the diode is reverse biased and behaves as an open.

✎ In this condition, the circuit behaves as a voltage divider with an output given by :

$$\text{Output voltage} \;=\; -\frac{R_L}{R + R_L} V_m$$

    Generally, R_L is much greater than R.   ∴   **Output voltage = - V_m**

✎ It may be noted that if it is desired to remove the negative half-cycle of the input, the only thing to be done is to reverse the polarities of the diode in the circuit shown in Fig. Such a clipper is then called a **negative clipper**.

♣ **(ii) BIASED CLIPPER: -**

✎ Sometimes it is desired to remove a small portion of positive or negative half-cycle of the signal voltage. For this purpose, biased clipper is used. Fig. shows the circuit of a biased clipper using a diode with a battery of V volts.
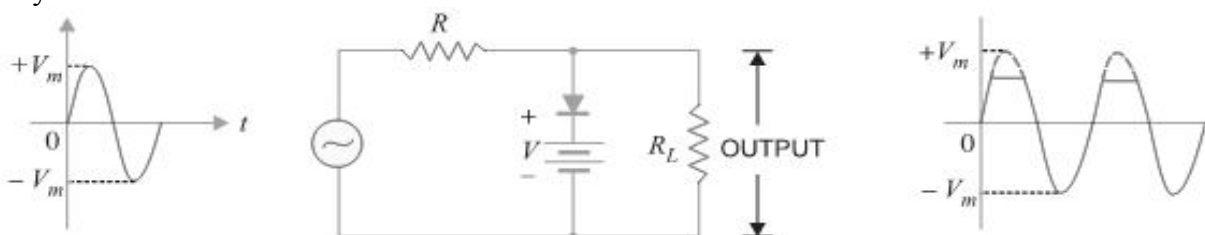

✎ With the polarities of battery shown, a portion of each positive half-cycle will be clipped. However, the negative half-cycles will appear as such across the load. Such a clipper is called *biased positive clipper*.

- ☙ The circuit action is as follows: - When input voltage is greater than +V, the diode behaves as a short and the output equals +V. The output will stay at +V so long as the input voltage is greater than +V.
- ☙ During the period the input voltage is less than +V, the diode is reverse biased and behaves as an open.
- ☙ Therefore, most of the input voltage appears across the output. In this way, the biased positive clipper removes input voltage above +V.
- ☙ During the negative half-cycle of the input voltage, the diode remains reverse biased. Therefore, almost entire negative half-cycle appears across the load.
- ☙ If it is desired to clip a portion of negative half-cycles of input voltage, the only thing to be done is to reverse the polarities of diode or battery. Such a circuit is then called a **biased negative clipper**.

♣ **(iii) COMBINATION CLIPPER: -**

- ☙ It is a combination of *biased positive* and *negative clippers*. With a combination clipper, a portion of both positive and negative half-cycles of input voltage can be removed or clipped as shown in Fig.
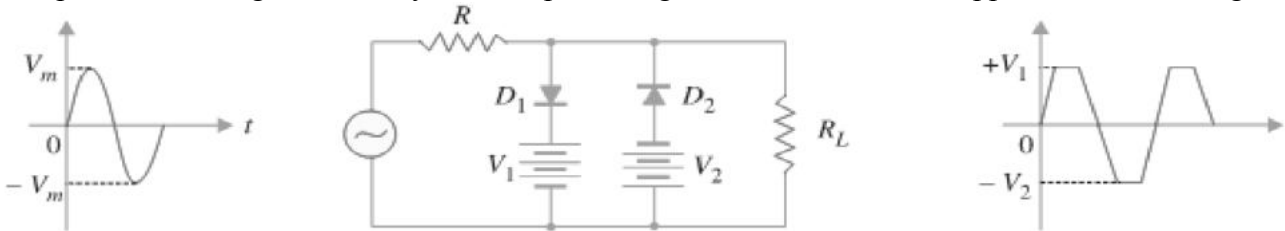
- ☙ The circuit action is as follows: - When positive input voltage is greater than $+V_1$, diode D_1 conducts heavily while diode D_2 remains reverse biased. Therefore, a voltage $+V_1$ appear across the load. This output stays at $+V_1$ so long as the input voltage exceeds $+V_1$
- ☙ On the other hand, during the negative half-cycle, the diode D_2 will conduct heavily and the output stays at $-V_2$ so long as the input voltage is greater than $-V_2$.
- ☙ Note that $+V_1$ and $-V_2$ are less than $+ V_m$ and $- V_m$ respectively.
- ☙ Between $+V_1$ and $-V_2$ neither diode is on. Therefore, in this condition, most of the input voltage appears across the load. It is interesting to note that this clipping circuit can give square wave output if V_m is much greater than the clipping levels.

♣ **APPLICATIONS OF CLIPPERS**

- ☙ **(i)** Changing the shape of a waveform **(ii)** Circuit transient(Sudden rise of Voltage or Current) protection

❖ **CLAMPING CIRCUITS: -**

- ☙ A circuit that places either the positive or negative peak of a signal at a desired d.c. level is known as a **clamping circuit.**

- ☙ A clamping circuit (or a clamper) essentially adds a d.c. component to the signal. Fig. shows the key idea behind clamping. The input signal is a sine wave having a peak-to-peak value of 10 V.
- ☙ The clamper adds the d.c. component and pushes the signal upwards so that the negative peaks fall on the zero level. As you can see, the waveform now has peak values of +10 V and 0 V.
- ☙ It may be seen that the shape of the original signal has not changed; only there is vertical shift in the signal. Such a clamper is called a **positive clamper**. The **negative clamper** does the reverse i.e. it pushes the signal downwards so that the positive peaks fall on the zero level.
- ☙ The following points may be noted carefully :
- ☙ **(i)** The clamping circuit **does not change the peak-to-peak or r.m.s. value** of the waveform. Thus referring to Fig. above, the input waveform and clamped output have the same peak-to-peak value i.e., 10 V in this case. If you measure the input voltage and clamped output with an a.c. voltmeter, the readings will be the same.
- ☙ **(ii)** A clamping circuit **changes the peak and average values** of a waveform. Thus in the above circuit, it is easy to see that input waveform has a peak value of 5 V and average value over a cycle is zero. The clamped output varies between 10 V and 0 V. Thus the peak value is 10 V and average value is 5 V.

♣ BASIC IDEA OF A CLAMPER

- ✎ A clamping circuit should not change peak-to-peak value of the signal; it should only change the dc level.
- ✎ To do so, a clamping circuit uses a capacitor, together with a diode and a load resistor R.
- ✎ Fig. shows the circuit of a *positive clamper*.
- ✎ The operation of a clamper is based on the principle that charging time of a capacitor is made very small as compared to its discharging time.
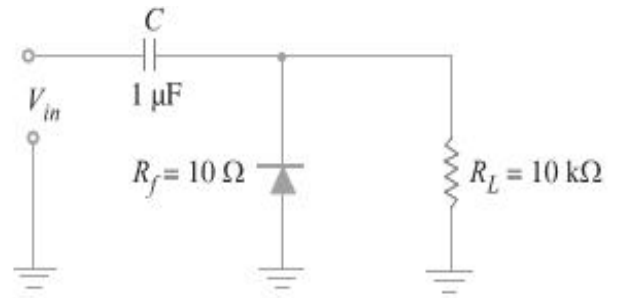
♣ POSITIVE CLAMPER: -

- ✎ Fig. shows the circuit of a positive clamper. The input signal is assumed to be a square wave with time period T. The clamped output is obtained across R_L.
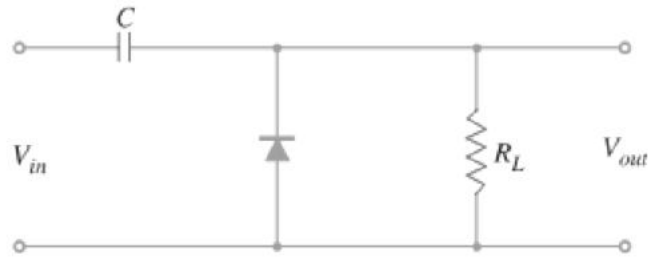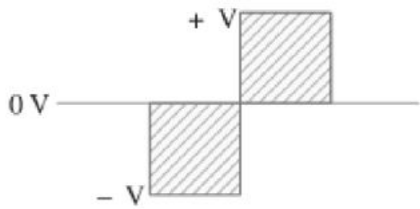
- ✎ The circuit design incorporates two main features.
- ✎ **Firstly**, the values of C and R_L are so selected that time constant $\tau = CR_L$ is very large.
- ✎ This means that voltage across the capacitor will not discharge significantly during the interval the diode is non-conducting.
- ✎ **Secondly**, R_LC time constant is deliberately made much greater than the time period T of the incoming signal.
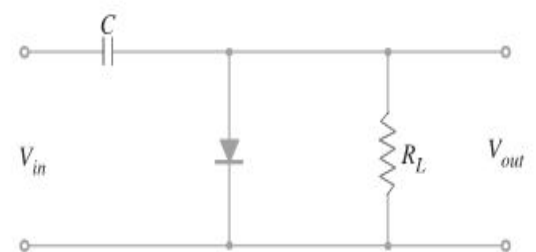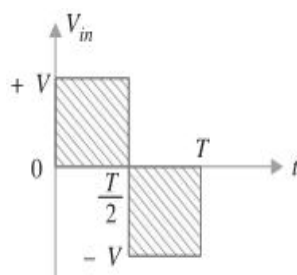
- ✎ **CIRCUIT OPERATION: -**
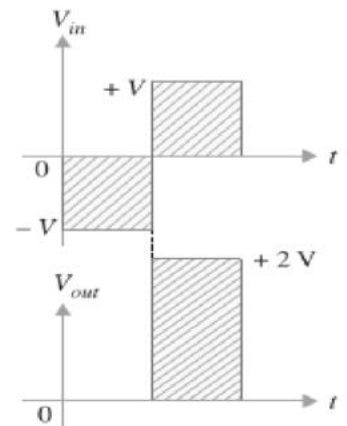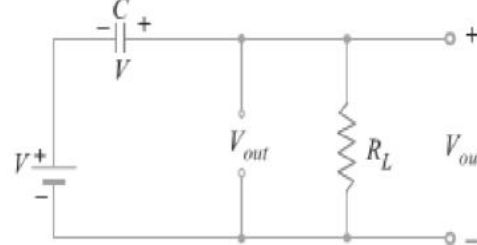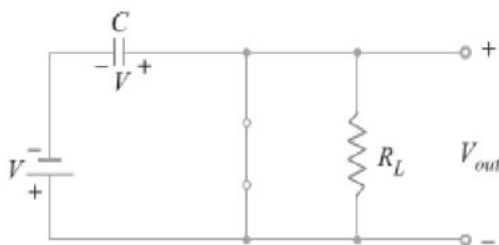
- ✎ **(i)** During the negative half-cycle of the input signal, the diode is forward biased. Therefore, the diode behaves as a short as shown in Fig (i). The charging time constant (= CR_f, where R_f=forward resistance of the diode) is very small so that the capacitor will charge to V volts very quickly.
- ✎ So, during this interval, the output voltage is directly across the short circuit. Therefore, **V_{out}= 0.**
- ✎ **(ii)** When the input switches to +V state (i.e., positive half-cycle), the diode is reverse biased and behaves as an open as shown in Fig (ii).
- ✎ Since the discharging time constant (= CR_L) is much greater than the time period of the input signal, the capacitor remains almost fully charged to V volts during the off time of the diode.
- ✎ Applying Kirchhoff 's voltage law in Fig (ii) to the input loop, we have, $V + V - V_{out} = 0$ **or** **V_{out}=2V**
- ✎ The resulting waveform is shown in Fig. (iii) It is clear that it is a positively clamped output. That is to say the input signal has been pushed upward by V volts so that negative peaks fall on the zero level.

♣ NEGATIVE CLAMPER: -

- ✎ Fig. shows the circuit of a negative clamper. The clamped output is taken across R_L.
- ✎ Note that only change from the positive clamper is that the connections of diode are reversed.

☙ **CIRCUIT OPERATION: -**

☙ **(i)** During the positive half-cycle of the input signal, the diode is forward biased. Therefore, the diode behaves as a short as shown in Fig (i).

☙ The charging time constant $(= CR_f)$ is very small so that the capacitor will charge to V volts very quickly. It is easy to see that during this interval, the output voltage is directly across the short circuit. Therefore, **Vout = 0**.
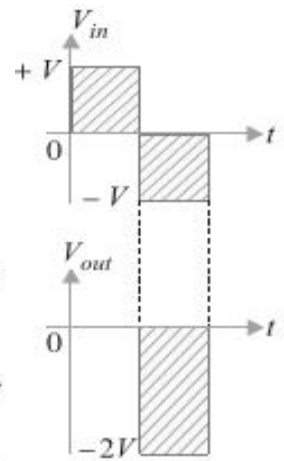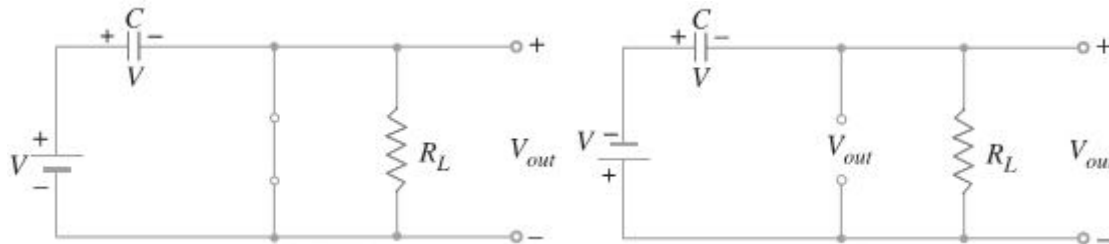
☙ **(ii)** When the input switches to –V state (i.e., negative half-cycle), the diode is reverse biased and behaves as an open as shown in Fig (ii).

☙ Since the discharging time constant $(= CR_L)$ is much greater than the time period of the input signal, the capacitor almost remains fully charged to V volts during the off time of the diode.

☙ Applying Kirchhoff 's voltage law to the input loop in Fig (ii) ➔   - V - V - V$_{out}$ = 0 **or   V$_{out}$ = - 2V**

☙ The resulting waveform is shown in Fig (iii). Note that total swing of the output signal is equal to the total swing of the input signal.

♣ **APPLICATIONS OF CLIPPERS**
   ✓ Clamper circuit is used TV receiver to restore the original d.c. reference signal to the video signal,
   ✓ Used to produce dc voltage multiple of peak ac input voltage i.e. known as **Voltage Multiplier.**

❖ **VOLTAGE MULTIPLIER**

☙ Voltage multiplier is a circuit, which produces an output dc voltage whose value is multiple of peak ac input voltage (i.e. $2V_m$, $3V_m$, $4V_m$ & so on).

☙ Such circuits are used as power supply for high voltage/low current device like CRO.

♣ **VOLTAGE DOUBLER: -**

☙ A voltage multiplier, whose output dc voltage is double the peak ac input voltage, is called a **Voltage Doubler.** Fig shows the circuit, of a half-wave voltage doubler.

☙ In this circuit, each section of a diode and capacitor (say D_1 and C_1 or D_2 and C_2) is called a *peak rectifier*. The operation of the circuit may be explained as given below:

☙ During the positive half-cycle of the input signal, the diode D_1 conducts (and diode D_2 is cut-off), charging the capacitor C_1 up to the peak rectified voltage (i.e., V_m).

☙ During the negative half-cycle, diode, D_1 is cut-off and diode D_2 conducts charging capacitor C_2.

☙ It may be noted that during negative half-cycle the voltage across capacitor C_1 is in series with the input voltage. Therefore the total voltage presented to capacitor C_2 is equal to $2V_m$.

☙ As a result of this, the capacitor C_2 is charged to a voltage of $2V_m$ during the negative half-cycle.

☙ On next positive half-cycle, the diode D_2 in non-conducting & capacitor will discharge through the load.

☙ If no load is connected across capacitor C_2, both capacitors stay charged at their full values (i.e., C_1 to V_m and C_2 to $2V_m$).

☙ It may be noted that both the diodes D_1 and D_2 have a peak inverse voltage (PIV) of $2V_m$ each.

☙ Fig (ii) shows another voltage doubler circuit known as full-wave voltage doubler.

☙ In this circuit during, the positive half cycle of a.c. input voltage, diode D_1 conducts charging capacitor C_1 to a peak voltage V_m with polarity as shown in the fig.
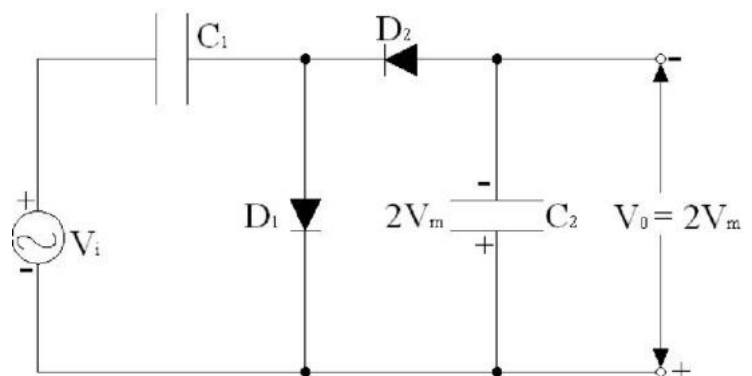
- ✎ The diode D_2 is cut-off at this time. During the negative half-cycle the diode D_2 conducts (while D_1 is at cut-off) charging capacitor C_2 to V_m.
- ✎ If there is no load connected across the output, then the output voltage is equal to $2V_m$.
- ✎ However if the load is connected, then the voltage would be less then $2V_m$.
- ✎ The peak inverse voltage (PIV) across each diode, in a full-wave voltage doubler, is equal to $2V_m$.
- ✎ The full-wave voltage doubler has an advantage over a convential center-tapped full-wave rectifier that it does not require any center-tapped transformer.
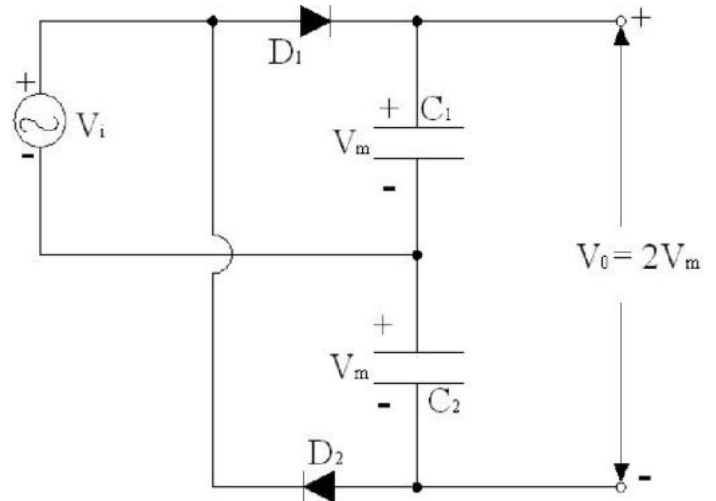
♣ VOLTAGE TRIPPLER AND QUADRUPLER: -

- ✎ Fig. shows the extension of a half-wave voltage doubler. This circuit develops an output voltage equal to 3 and 4 times the peak input voltage.
- ✎ It is obvious from the pattern of the circuit connection as to how additional diodes and capacitors may be connected for the amount of voltage multiplication.
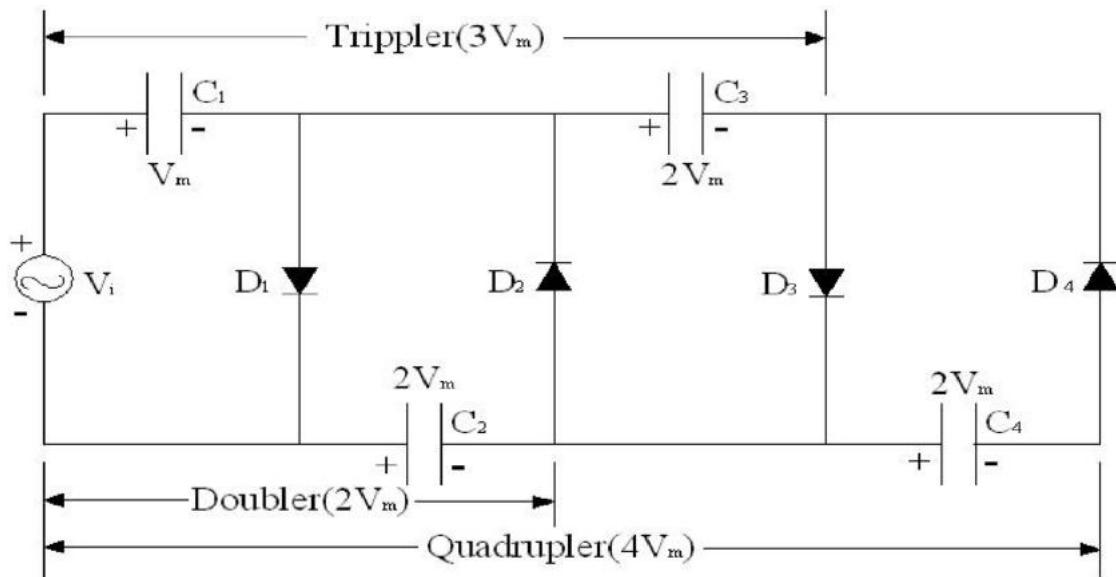
- ✎ But it has been observed that if we increase the voltage multiplication beyond four, the regulation is very poor. It is because of this fact, that voltage multipliers are not used in low-voltage supplies.
- ✎ The operation of the voltage Tripler and quadrupler circuit may be understood from the fact, that during the first positive half-cycle, the capacitor C_1 charges through diode D_1 to a peak voltage V_m.
- ✎ During the negative half-cycle, capacitor C_2 charges through diode D_2 to twice the peak voltage $2V_m$ developed by the sum of the voltage across capacitor C_1 and the input signal.
- ✎ During the second positive half-cycle, the diode D_3 conducts and the voltage across capacitor C_2 charges the capacitor C_3 to the same $2V_m$ peak voltage
- ✎ During the negative half-cycle, diodes D_2 and D_4 conduct allowing capacitor C_3 to charge capacitor C_4 to the same $2V_m$ peak voltage.
- ✎ It is evident from fig. that the voltage across capacitor C_2 is $2V_m$, across C_1 and C_3 is $3V_m$ and across C_2 and C_4 is $4V_m$.
- ✎ It means that the voltage quadrupler circuit can provide three different voltages i.e. $2V_m$, $3V_m$, $4V_m$.
- ✎ It will be interesting to know that if we use additional section of diode and capacitor with the voltage quadrupler circuit, then each capacitor will be charged to $2V_m$.
- ✎ The peak inverse voltage for each diode in the circuit is equal to $2V_m$.

❖ MULTIVIBRATORS: -

✍ An electronic circuit that generates square waves (or other non-sinusoidal such as rectangular, saw-tooth waves) is known as a **multivibrator.**

✍ A multivibrator is a switching circuit which depends for operation on positive feedback. It is basically a two-stage amplifier with output of one feedback to the input of the other as shown in Fig (i).
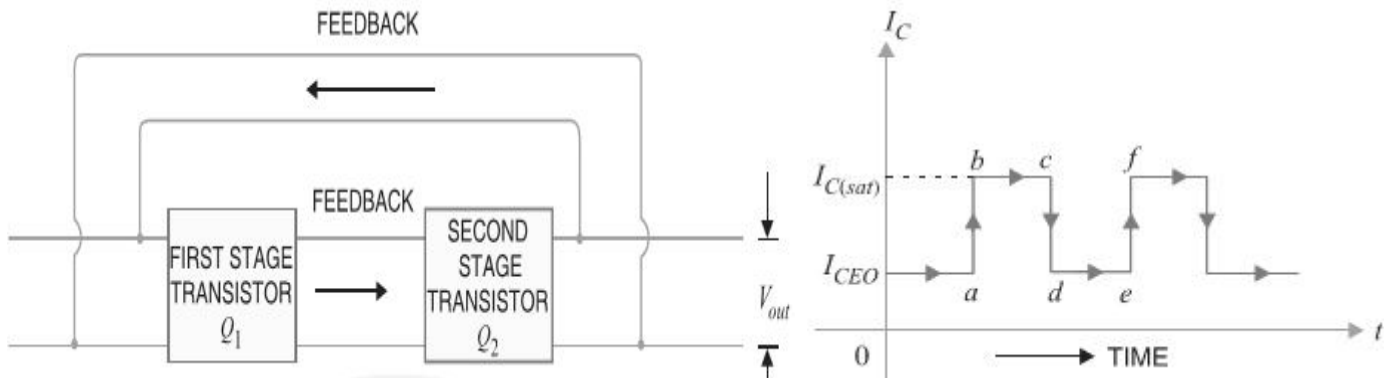

✍ The name multivibrator is derived from the fact that a square wave actually consists of a large number of (Fourier series analysis) sinusoidal of different frequencies.

✍ The circuit operates in two states (viz ON and OFF) controlled by circuit conditions. Each amplifier stage supplies feedback to the other in such a manner that will drive the transistor of one stage to saturation (ON state) and the other to cut off (OFF state).

✍ After a certain time controlled by circuit conditions, the action is reversed i.e. saturated stage is driven to cut off and the cut off stage is driven to saturation. The output can be taken across either stage and may be rectangular or square wave depending upon the circuit conditions.

✍ Fig (ii) shows the block diagram of a multivibrator. It is a two-stage amplifier with 100% positive feedback. Suppose output is taken across the transistor Q_2. At any particular instant, one transistor is ON and conducts I_C (sat) while the other is OFF. Suppose Q_2 is ON and Q_1 is OFF.

✍ The collector current in Q_2 will be I_C (sat) as shown in Fig (ii). This condition will prevail for a time (bc in this case) determined by circuit conditions.

✍ After this time, transistor Q_2 is cut off and Q_1 is turned ON. The collector current in Q_2 is now I_{CEO} as shown. The circuit will stay in this condition for a time de. Again Q_2 is turned ON and Q_1 is driven to cut off. In this way, the output will be a square wave.

♣ TYPES OF MULTIVIBRATORS: -

✍ A multivibrator is basically a two-stage amplifier with output of one feedback to the input of the other.

✍ At any particular instant, one transistor is ON and the other is OFF. After a certain time depending upon the circuit components, the stages reverse their conditions.

✍ The conducting stage suddenly cuts off and the non-conducting stage suddenly starts to conduct.

✍ The two possible states of a multivibrator are :

✍ Depending upon the manner in which the two stages interchange their states, the multivibrators are classified as :-

	ON	OFF
First State	Q_1	Q_2
Second State	Q_2	Q_1

✓ Astable or free running multivibrator

✓ Monostable or one-shot multivibrator

✓ Bi-stable or flip-flop multivibrator

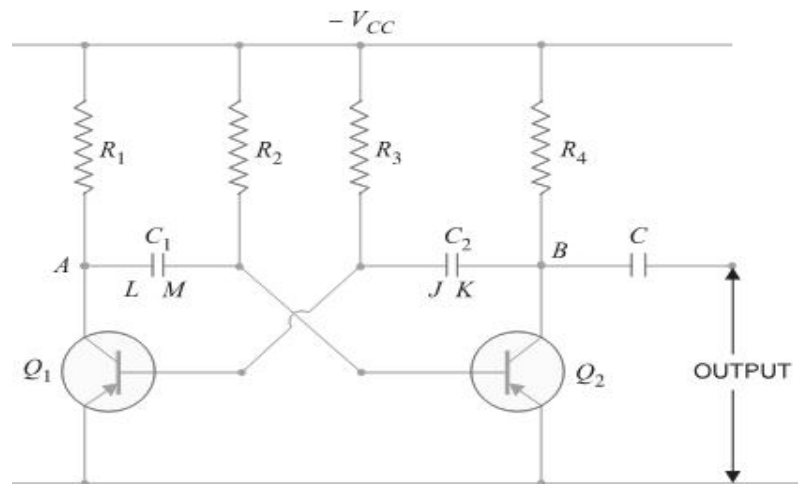✍ Fig. shows the input/output relations for the three types of multivibrators.
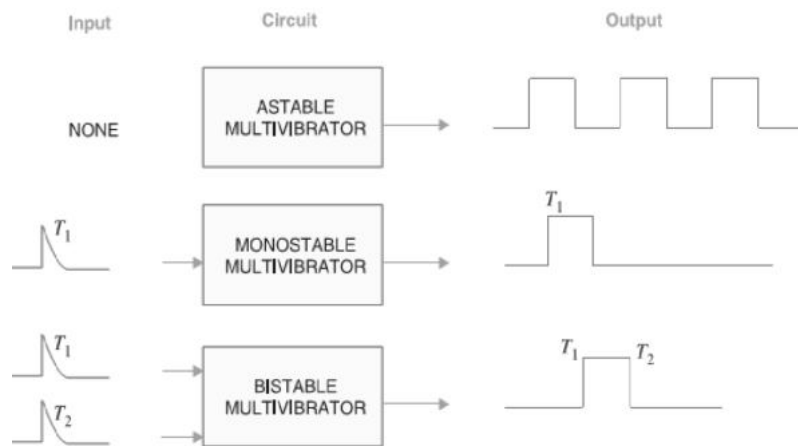
✍ **(i)** The astable or free running multivibrator alternates automatically between the two states and remains in each for a time dependent upon the circuit constants.

✍ Thus it is just an oscillator since it requires no external pulse for its operation.

- Of course, it does require a source of d.c. power. Because it continuously produces the square-wave output, it is often referred to as a free running multivibrator.
- **(ii)** The monostable or one-shot multivibrator has one state stable and one quasi-stable (i.e. half-stable) state. The application of input pulse triggers the circuit into its quasi-stable state, in which it remains for a period determined by circuit constants.
- After this period of time, the circuit returns to its initial stable state, the process is repeated upon the application of each trigger pulse.
- Since the monostable multivibrator produces a single output pulse for each input trigger pulse, it is generally called one-shot multivibrator.
- **(iii)** The bistable multivibrator has both the two states stable. It requires the application of an external triggering pulse to change the operation from either one state to the other.
- Thus one pulse is used to generate half-cycle of square wave and another pulse to generate the next half-cycle of square wave. It is also known as a **flip-flop multivibrator** because of the two possible states it can assume.

❖ TRANSISTOR ASTABLE MULTIVIBRATOR

- A multivibrator which generates square waves of its own (i.e. without any external triggering pulse) is known as an **astable** or **free running multivibrator.**

- The astable multivibrator has no stable state. It switches back and forth from one state to the other, remaining in each state for a time determined by circuit constants.
- In other words, at first one transistor conducts (i.e. ON state) and the other stays in the OFF state for some time.
- After this period of time, the second transistor is automatically turned ON and the first transistor is turned OFF.
- Thus the multivibrator will generate a square wave output of its own.
- The width of the square wave and its frequency will depend upon the circuit constants.
- ❖ **CIRCUIT DETAILS: -** Fig. shows the circuit of a typical transistor astable multivibrator using two identical transistors Q_1 and Q_2.
- The circuit essentially consists of two symmetrical CE amplifier stages, each providing a feedback to the other. Thus *collector loads* of the two stages are equal i.e. $R_1 = R_4$ and the *biasing resistors* are also equal i.e. $R_2 = R_3$.
- The output of transistor Q_1 is coupled to the input of Q_2 through C_1 while the output of Q_2 is fed to the input of Q_1 through C_2. The square wave output can be taken from Q_1 or Q_2.
- ❖ **CIRCUIT OPERATION: -** When V_{CC} is applied, collector currents start flowing in Q_1 and Q_2. In addition, the coupling capacitors C_1 and C_2 also start charging up.

- As the characteristics of no two transistors (i.e. β, V_{BE}) are exactly alike, therefore, one transistor, say Q_1, will conduct more rapidly than the other.
- The rising collector current in Q_1 drives its collector more and more positive. The increasing positive output at point A is applied to the base of transistor Q_2 through C_1.
- This establishes a reverse bias on Q_2 and its collector current starts decreasing. As the collector of Q_2 is connected to the base of Q_1 through C_2, therefore, base of Q_1 becomes more negative i.e. Q_1 is more forward biased.
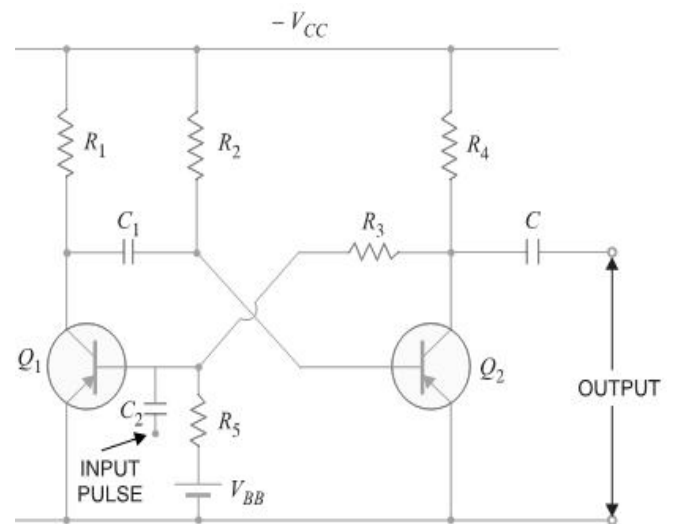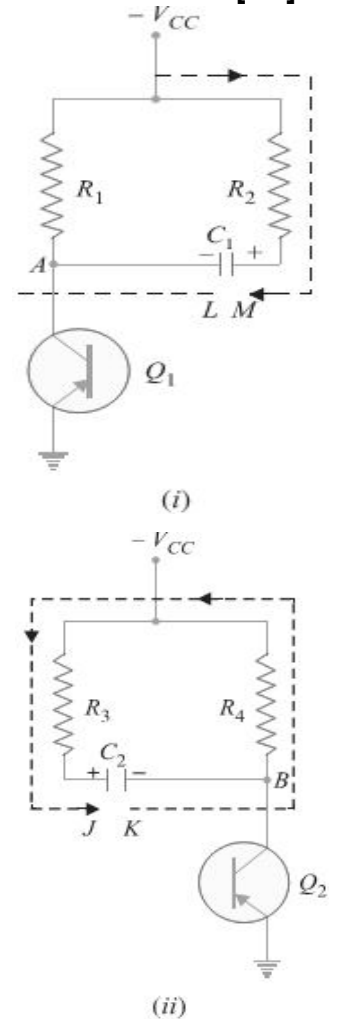- This further increases the collector current in Q_1 and causes a further decrease of collector current in Q_2. This series of actions is repeated until the circuit drives Q_1 to saturation and Q_2 to cut off.
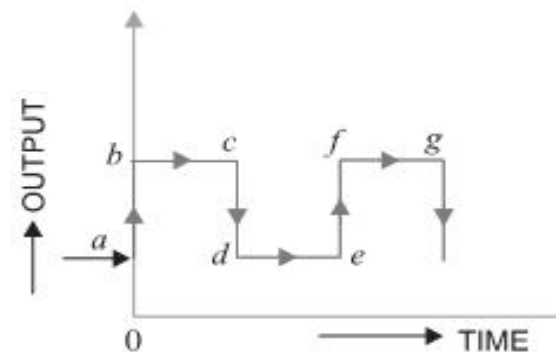
- These actions occur very rapidly and may be considered practically instantaneous. The output of Q_1 (ON state) is approximately zero and that of Q_2 (OFF state) is approximately V_{CC}.

- This is shown by ab in above Fig. When Q_1 is at saturation and Q_2 is cut off, the full voltage V_{CC} appears across R_1 and voltage across R_4 will be zero.

- The charges developed across C_1 and C_2 are sufficient to maintain the saturation and cut off conditions at Q_1 and Q_2 respectively. This condition is represented by time interval bc in Fig.

- However, the capacitors will not retain the charges indefinitely but will discharge through their respective circuits. The discharge path for C_1, with plate L negative and Q_1 conducting, is $LAQ_1V_{CC}R_2M$ as shown in Fig. (i).

- The discharge path for C_2, with plate K negative and Q_2 cut off, is KBR_4R_3J as shown in Fig (ii). As the resistance of the discharge path for C_1 is lower than that of C_2, therefore, C_1 will discharge more rapidly.

- As C_1 discharges, the base bias at Q_2 becomes less positive and at a time determined by R_2 and C_1, forward bias is re-established at Q_2. This causes the collector current to start in Q_2.

- The increasing positive potential at collector of Q_2 is applied to the base of Q_1 through the capacitor C_2. Hence the base of Q_1 will become more positive i.e. Q_1 is reverse biased.

- The decrease in collector current in Q_1 sends a negative voltage to the base of Q_2 through C_1, thereby causing further increase in the collector current of Q_2.

- With this set of actions taking place, Q_2 is quickly driven to saturation and Q_1 to cut off. This condition is represented by cd in Fig. The period of time during which Q_2 remains at saturation and Q_1 at cut off is determined by C_2 and R_3.


(i)

(ii)

❖ TRANSISTOR MONOSTABLE MULTIVIBRATOR

- A multivibrator in which one transistor is always conducting (i.e. in the ON state) and the other is non-conducting (i.e. in the OFF state) is called a **monostable multivibrator**

- A monostable multivibrator has only one state stable. In other words, if one transistor is conducting and the other is non-conducting, the circuit will remain in this position.

- It is only with the application of external pulse that the circuit will interchange the states.

- However, after a certain time, the circuit will automatically switch back to the original stable state and remains there until another pulse is applied.

- Thus a monostable multivibrator cannot generate square waves of its own like an astable multivibrator. Only external pulse will cause it to generate the square wave.

❖ CIRCUIT DETAILS: -

- Fig. shows the circuit of a transistor monostable multivibrator. It consists of two similar transistors Q_1 and Q_2 with equal collector loads i.e. $R_1 = R_4$.

- The values of V_{BB} and R_5 are such as to reverse bias Q_1 and keep it at cut off. The collector supply V_{CC} and R_2 forward bias Q_2 and keep it at saturation.

- The input pulse is given through C_2 to obtain the square wave. Again output can be taken from Q_1 or Q_2.

❖ CIRCUIT OPERATION: -

- With the circuit arrangement shown, Q_1 is at cut off and Q_2 is at saturation. This is the stable state for the circuit and it will continue to stay in this state until a triggering pulse is applied at C_2.

- When a negative pulse of short duration and sufficient magnitude is applied to the base of Q_1 through C_2, the transistor Q_1 starts conducting and positive potential is established at its collector.

- The positive potential at the collector of Q_1 is coupled to the base of Q_2 through capacitor C_1. This decreases the forward bias on Q_2 and its collector current decreases.
- The increasing negative potential on the collector of Q_2 is applied to the base of Q_1 through R_3. This further increases the forward bias on Q_1 and hence its collector current.
- With this set of actions taking place, Q_1 is quickly driven to saturation and Q_2 to cut off. With Q_1 at saturation and Q_2 at cut off, the circuit will come back to the original stage (i.e. Q_2 at saturation and Q_1 at cut off) after some time as explained in the following discussion.
- The capacitor C_1 (charged to approximately V_{CC}) discharges through the path $R_2 V_{CC} Q_1$. As C_1 discharges, it sends a voltage to the base of Q_2 to make it less positive.
- This goes on until a point is reached when forward bias is re-established on Q_2 and collector current starts to flow in Q_2.
- The step by step events already explained occur and Q_2 is quickly driven to saturation and Q_1 to cut off.
- This is the stable state for the circuit and it remains in this condition until another pulse causes the circuit to switch over the states.

❖ TRANSISTOR BISTABLE MULTIVIBRATOR: -
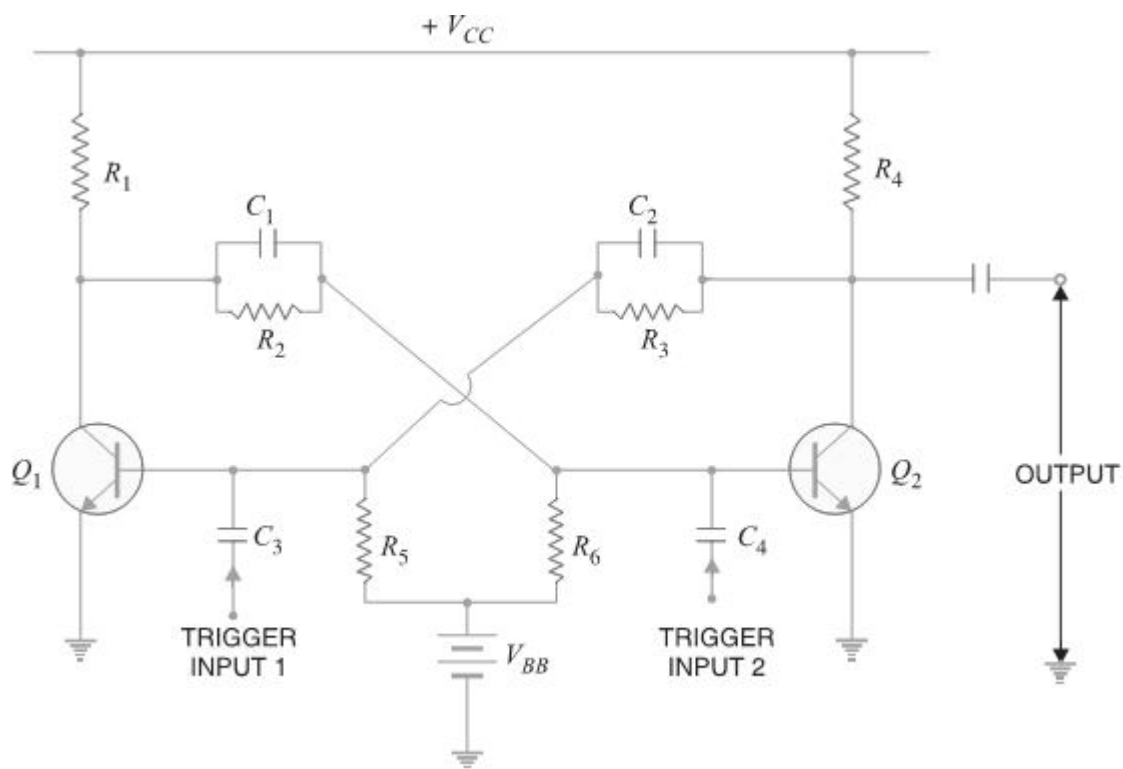
- A multivibrator which has both the states stable is called a **Bistable Multivibrator.**
- The bistable multivibrator has both the states stable. It will remain in whichever state it happens to be until a trigger pulse causes it to switch to the other state.
- For instance, suppose at any particular instant, transistor Q_1 is conducting and transistor Q_2 is at cut off. If left to itself, the bistable multivibrator will stay in this position forever.
- However, if an external pulse is applied to the circuit in such a way that Q_1 is cut off and Q_2 is turned on, the circuit will stay in the new position.
- Another trigger pulse is then required to switch the circuit back to its original state.

❖ CIRCUIT DETAILS: -

- Circuit details. Fig. shows the circuit of a typical transistor bistable multivibrator.
- It consists of two identical CE amplifier stages with output of one fed to the input of the other.
- The feedback is coupled through resistors (R_2, R_3) shunted by capacitors C_1 and C_2.
- The main purpose of capacitors C_1 and C_2 is to improve the switching characteristics of the circuit by passing the high frequency components of the square wave.
- This allows fast rise and fall times and hence distortion less square wave output. The output can be taken across either transistor.

❖ **OPERATION: -**

❧ When V_{CC} is applied, one transistor will start conducting slightly ahead of the other due to some differences in the characteristics of the transistors.

❧ This will drive one transistor to saturation and the other to cut off in a manner described for the astable multivibrator.

❧ Assume that Q_1 is turned ON and Q_2 is cut OFF. If left to itself, the circuit will stay in this condition. In order to switch the multivibrator to its other state, a trigger pulse must be applied.

❧ A negative pulse applied to the base of Q_1 through C_3 will cut it off or a positive pulse applied to the base of Q_2 through C_4 will cause it to conduct.

❧ Suppose a negative pulse of sufficient magnitude is applied to the base of Q_1 through C_3.

❧ This will reduce the forward bias on Q_1 and cause a decrease in its collector current and an increase in collector voltage.

❧ The rising collector voltage is coupled to base of Q_2 where it forward biases base-emitter junction of Q_2.

❧ This will cause an increase in its collector current and decrease in collector voltage.

❧ The decreasing collector voltage is applied to the base of Q_1 where it further reverse biases the base-emitter junction of Q_1 to decrease its collector current.

❧ With this set of actions taking place, Q_2 is quickly driven to saturation and Q_1 to cut off.

❧ The circuit will now remain stable in this state until a negative trigger pulse at Q_2 (or a positive trigger pulse at Q_1) changes this state.
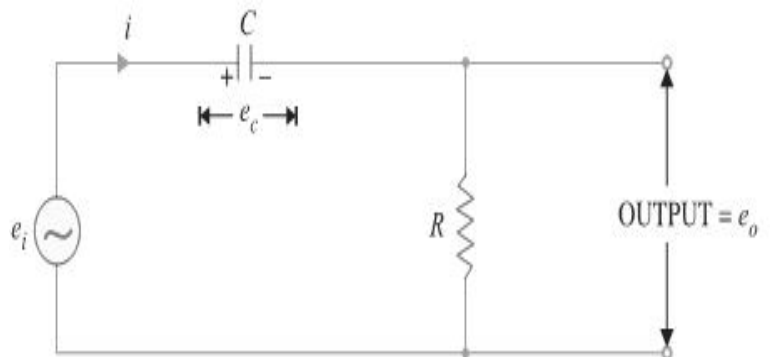
❖ <u>DIFFERENTIATING CIRCUIT:</u>

❧ A circuit in which output voltage is directly proportional to the derivative of the input is known as a **Differentiating Circuit.**

> i. e.   **Output ∝ d/dt (Input)**

❧ A differentiating circuit is a simple RC series circuit with output taken across the resistor R.

❧ The circuit is suitably designed so that output is proportional to the derivative of the input.

❧ Thus if a d.c. or constant input is applied to such a circuit, the output will be zero. It is because the derivative of a constant is zero.

❧ Fig shows a typical differentiating circuit. The output across R will be the derivative of the input.

❧ It is important to note that merely using voltage across R does not make the circuit a differentiator; it is also necessary to set the proper circuit values.

❧ In order to achieve good differentiation, the following two conditions should be satisfied :

♣ The time constant RC of the circuit should be much smaller than the time period of the input wave.

♣ The value of X_C should be 10 or more times larger than R at the operating frequency.

❧ Fulfilled these conditions, the output across R in Fig. will be the derivative of the input.

Let e_i be the input alternating voltage and let i be the resulting alternating current.

The charge q on the capacitor at any instant is   **q = C e_c**

Now $i = \dfrac{dq}{dt} = \dfrac{d}{dt} q = \dfrac{d}{dt} (C\, e_c)$

$i = C . \dfrac{d}{dt} e_c$

❧ Since the capacitive reactance is very much larger than R, the input voltage can be considered equal to the capacitor voltage with negligible error i.e. **$e_c = e_i$**

∴ $i = C . \dfrac{d}{dt} e_i$

❧ Output voltage, $e_o = i\, R = R\, C . \dfrac{d}{dt} e_i$ ➔ $e_o \propto \dfrac{d}{dt} (e_i)$

➔ **Output Voltage ∝ d/dt (Input Voltage)**

❖ **OUTPUT WAVEFORMS: -**

✎ The output waveform from a differentiating circuit depends upon the time constant and shape of the input wave. Three important cases will be considered.

✎ **(i) When input is a square wave: -** In this case, output will consist of sharp narrow pulses as shown in Fig. During the OC part of input wave, its amplitude changes abruptly and hence the differentiated wave will be a sharp narrow pulse as shown in Fig.
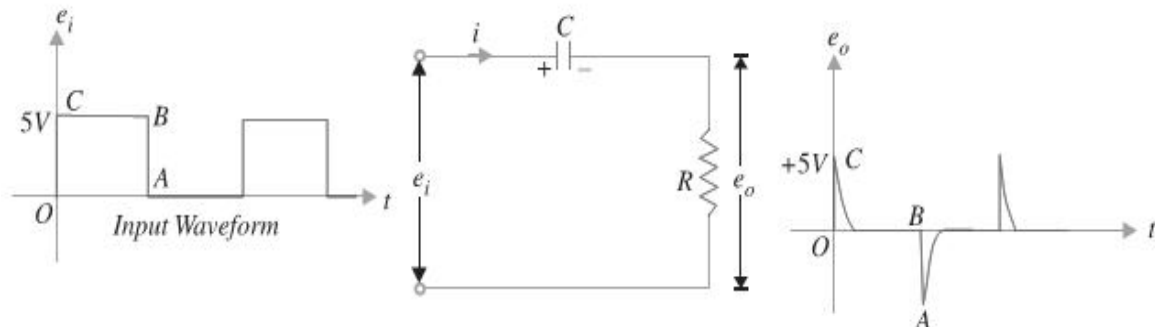
✎ However, during the constant part CB of the input, the output will be zero because derivative of a constant is zero. Let us look at the physical explanation of this behavior of the circuit.

✎ Since time constant RC of the circuit is very small w.r.t. time period of input wave and $X_C \gg R$, the capacitor will become fully charged during the early part of each half-cycle of the input wave.

✎ During the remainder part of the half-cycle, the output of the circuit will be zero because the capacitor voltage (e_c) neutralizes the input voltage and there can be no current flow through R.

✎ Thus we shall get sharp pulse at the output during the start of each half-cycle of input wave while for the remainder part of the half-cycle of input wave, the output will be zero.

✎ In this way, a symmetrical output wave with sharp positive and negative peaks is produced. Such pulses are used in many ways in electronic circuits e.g. in television transmitters and receivers, in multivibrators to initiate action etc.

✎ **(ii) When input is a triangular wave:-** When the input fed to a differentiating circuit is a triangular wave, the output will be a rectangular wave as shown in Fig.

✎ During the period OA of the input wave, its amplitude changes at a constant rate and, therefore, the differentiated wave has a constant value for each constant rate of change.

✎ During the period AB of the input wave, the change is less abrupt so that the output will be a very narrow pulse of rectangular form.

✎ Thus when a triangular wave is fed to a differentiating circuit, the output consists of a succession of rectangular waves of equal or unequal duration depending upon the shape of the input wave.
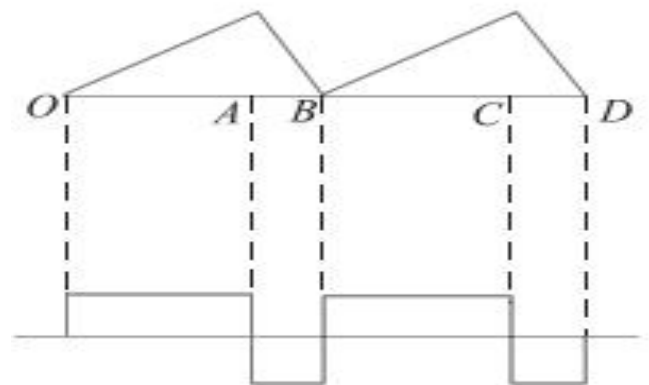
✎ **(iii) When input is a sine wave.** A sine wave input becomes a cosine wave and a cosine wave input becomes an inverted sine wave at the output.

❖ **APPLICATIONS OF DIFFERENTIATING CIRCUIT : -**

♣ To generate a series of narrow pulses from rectangular or square waves.

♣ To generate a step from a ramp input.

♣ To generate a square wave from triangular wave inputs.

❖ # INTEGRATING CIRCUIT: -

✎ A circuit in which output voltage is directly proportional to the integral of the input is known as an **Integrating Circuit.**

i. e.   **Output ∫ (Input)**

✎ An integrating circuit is a simple RC series circuit with output taken across the capacitor C as shown in Fig. It may be seen that R and C of the differentiating circuit have changed places.

- In order that the circuit renders good integration, the following conditions should be fulfilled :
- ♣ The time constant RC of the circuit should be very large as compared to the time period of input wave.
- ♣ The value of R should be 10 or more times larger than X_C.
- Let e_i be the input alternating voltage and let i be the resulting alternating current.
- Since R is very large as compared to capacitive reactance X_C of the capacitor, it is reasonable to assume that voltage across R (i.e. e_R) is equal to the input voltage i.e.
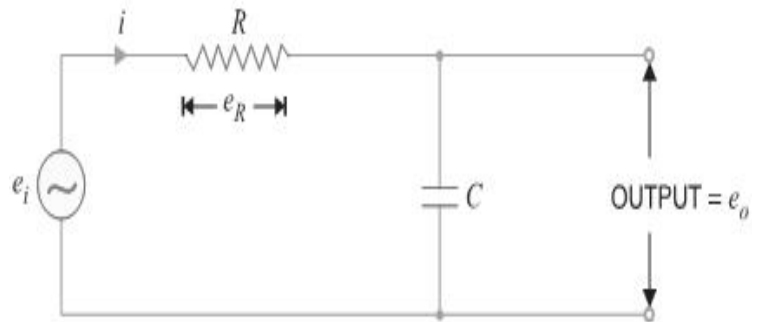
$$\textbf{e}_\textbf{i} = \textbf{e}_\textbf{R} \quad , \quad \text{Also} \quad i = \frac{e_R}{R} = \frac{e_i}{R}$$

- The charge q on the capacitor at any instant is $\quad \textbf{q} = \int \textbf{i} \, \textbf{dt} = \int \frac{e_i}{R} \, dt$

- Output voltage, $\quad e_o = \frac{q}{C} = \frac{\int \frac{e_i}{R} dt}{C}$

$$= \frac{1}{RC} \int e_i \, dt$$

$$= \text{constant} \quad \textbf{x} \quad \int e_i \, dt$$

➔ $e_o \propto \int e_i \, dt$

∴ **Output voltage** $\propto \int$ **Input**

❖ **OUTPUT WAVEFORMS: -**

- The output waveform from an integrating circuit depends upon time constant and shape of the input wave. Two important cases will be discussed:
- **(i) When input is a square wave: -** When the input fed to an integrating circuit is a square wave, the output will be a triangular wave as shown in Fig. (i).
- As integration means summation, therefore, output from an integrating circuit will be the sum of all the input waves at any instant.
- This sum is zero at A and goes on increasing till it becomes maximum at C. After this, the summation goes on decreasing to the onset of negative movement CD of the input.
- **(ii) When input is rectangular wave: -** When the input fed to an integrating circuit is a rectangular wave, the output will be a triangular wave as shown in Fig. (ii).

(i)

(ii)
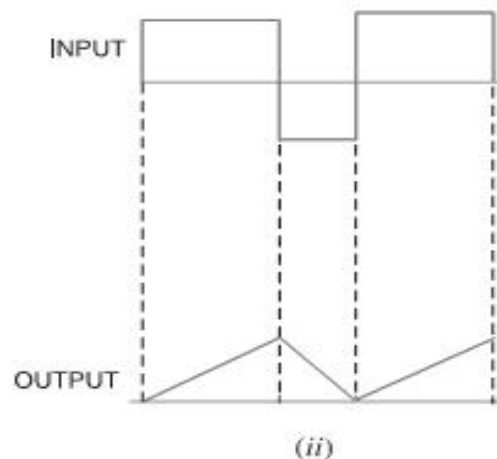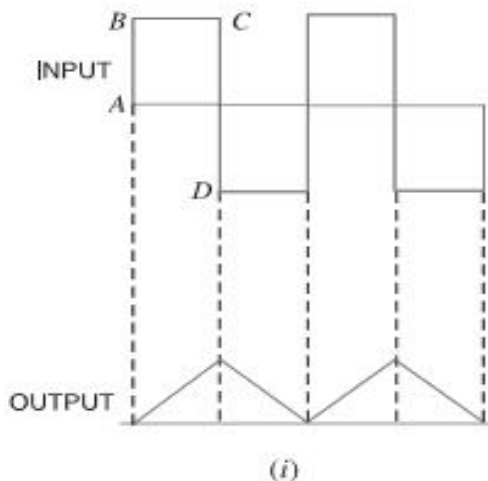
❖ **APPLICATIONS OF INTEGRATING CIRCUIT : -**

- ♣ To perform mathematical integration in analog computers.
- ♣ To generate a triangular wave from a square waves.
- ♣ To generate a saw tooth wave from a rectangular wave.
- **Differentiator** is an RC circuit with an input applied to the Capacitor and output taken across Resistor.
- **Integrator** is an RC circuit with an input applied to the Resistor and output taken across Capacitor.
- **Time Constant** is the product of R & C.