Badriprasad Institute of Technology, Sambalpur

Lesson plan for Theory -3, MICROPROCESSOR & MICROCONTROLLER

Semester & Branch : 4TH SEM, ETC Engineering **Total Periods-75**

Name of the faculty : MR. MALAYA BASANT TRIPATHY **No of periods /week-5**

WEEK	CLASS DAY	THEORY
1ST	1ST	INTRODUCTION TO MICROPROCESSOR & MICROCONTROLLER
	2ND	DISTINGUISH BETWEEN MICROPROCESSOR & MICROCONTROLLER
	3RD	CONCEPT OF ADDRESS BUS, DATA BUS
	4TH	CONTROL BUS & SYSTEM BUS
	5TH	GENERAL BLOCK STRUCTURE BLOCK DIAGRAM
2ND	1ST	BASIC ARCHITECTURE OF 8085 MICROPROCESSOR CONTD..
	2ND	BASIC ARCHITECTURE OF 8085 MICROPROCESSOR
	3RD	SIGNAL DESCRIPTION OF 8085 MICROPROCESSOR
	4TH	REGISTER ORGANIZATIONS
	5TH	DISTINGUISH BETWEEN SPR & GPR
3RD	1ST	TIMING & CONTROL MODULE
	2ND	STACK, STACK POINTER, STACK TOP
	3RD	INTERRUPTS OF 8085
	4TH	MASKING OF INTERRUPTS(SIM, RIM)
	5TH	ADDRESSING DATA
4TH	1ST	DIFFERENTIATE BETWEEN ONE-BYTE, TWO BYTE, THREE BYTE INSTRUCTIONS
	2ND	ADDRESSING MODES
	3RD	INSTRUCTION SET OF 8085 MICROPROCESSOR CONTD..
	4TH	INSTRUCTION SET OF 8085 MICROPROCESSOR
	5TH	SIMPLE ASSEMBLY LANGUAGE PROGRAMMING OF 8085- SIMPLE ADDITION & SUBSTRACTION
5TH	1ST	LOGIC OPERATIONS
	2ND	COUNTERS & TIME DELAY
	3RD	LOOPING, COUNTING, INDEXING
	4TH	STACK & SUBROUTINE PROGRAMS
	5TH	CODE CONVERSION, BCD ARITHMETIC, BLOCK TRANSFER
6TH	1ST	COMPARE BETWEENT TWO NUMBERS
	2ND	ARRAY HANDLING
	3RD	MEMORY ADDRESSING
	4TH	I/O ADDRESSING
	5TH	OPCODE, OPERAND, T-STATES
7TH	1ST	FETCH CYCLE, MACHINE CYCLE
	2ND	INSTRUCTION CYCLE & TIMING DIAGRAM
	3RD	TIMING DIAGRAM FOR MEMORY READ/WRITE
	4TH	TIMING DIAGRAM FOR I/O READ & WRITE
	5TH	TIMING DIAGRAM FOR 8085 INSTRUCTION(MOV,MVI,LDA INSTRUCTION)
8TH	1ST	CONCEPT OF INTERFACING
	2ND	MEMORY MAPPING & I/O MAPPING
	3RD	INTERFACING EPROM & RAM MEMORIES
	4TH	ADDRESS DECODING OF I/O DEVICE
	5TH	PROGRAMMABLE PERIPHERAL INTERFACE-8255
9TH	1ST	ADC & DAC WITH INTERFACING
	2ND	INTERFACING SEVEN SEGMENT DISPLAY
	3RD	GENERATE SQUARE WAVE ON ALL LINES OF 8255
	4TH	INTERFACE A TRAFFIC LIGHT CONTROLLER USING 8255
	5TH	INTERFACE OF STEPPER MOTOR CONTROL USING 8255
10TH	1ST	DMA CONTROLLER
	2ND	USART EXPLANATION
	3RD	REGISTER ORGANIZATION OF 8086

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	4TH	INTEL ARCHITECTURE OF 8086 CONTD..
	5TH	INTEL ARCHITECTURE OF 8086
11TH	1ST	SIGNAL DESCRIPTION OF 8086
	2ND	GENERAL BUS OPERATION
	3RD	PHYSICAL MEMORY ORGANIZATION
	4TH	MINIMUM MODE & TIMINGS
	5TH	MAXIMUM MODE & TIMINGS
12TH	1ST	MASKING OF INTERRUPTS(SIM, RIM)
	2ND	NON-MASKABLE & MASKABLE INTERRUPT
	3RD	PROGRAMMABLE PERIPHERAL INTERFACE-8255
	4TH	8086 INSTRUCTION SET
	5TH	ADDRESSING MODES
13TH	1ST	ASSEMBLER DIRECTIVES & OPERATORS
	2ND	ASSEMBLY LANGUAGE PROGRAMMING OF 8086 MICROPROCESSOR
	3RD	DISTINGUISH BETWEEN MICROPROCESSOR & MICROCONTROLLER
	4TH	8 BIT & 16 BIT MICROCONTROLLER
	5TH	CISC & RISC PROCESSOR
14TH	1ST	ARCHITECTURE OF 8051 MICROCONTROLLER
	2ND	SIGNAL DESCRIPTION OF 8051 MICROCONTROLLER
	3RD	RAM STRUCTURE, SFR
	4TH	REGISTERS, TIMERS
	5TH	INTERRUPTS OF 8051 CONTROLLER
15TH	1ST	ADDRESSING MODES OF 8051 MICROCONTROLLER, ASSEMBLY LANGUAGE PROGRAMMING
	2ND	SERIAL COMMUNICATION, INTERRUPTS & INTERFACING 8255
	3RD	OBJECTIVE TYPE QUESTION DISCUSSION
	4TH	SEMESTER PATTERN QUESTION DISCUSSION
	5TH	PRACTICE TEST

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